N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package
			TO-92
60V	5.0Ω	0.75A	VN10KN3

Features

- ❑ Free from secondary breakdown
- ❑ Low power drive requirement
- ❑ Ease of paralleling
- ❑ Low C_{ISS} and fast switching speeds
- ❑ Excellent thermal stability
- ❑ Integral Source-Drain diode
- ❑ High input impedance and high gain
- ❑ Complementary N- and P-channel devices

Applications

- ❑ Motor controls
- ❑ Converters
- ❑ Amplifiers
- ❑ Switches
- ❑ Power supply circuits
- ❑ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Option

S G D

TO-92

Note: See Package Outline section for dimensions.

11/12/01

Thermal Characteristics

Package	I_D (continuous)[1,2]	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}
TO-92	0.31A	1.0A	1.0W	125	170	0.31A	1.0A

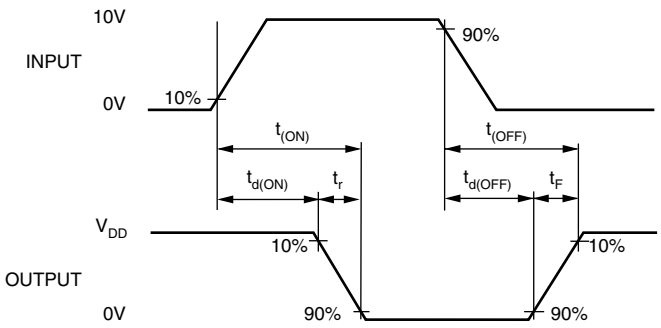
Notes:
1. I_D (continuous) is limited by max rated T_j.
2. VN0106N3 can be used if an I_D (continuous) of 0.5 is needed.

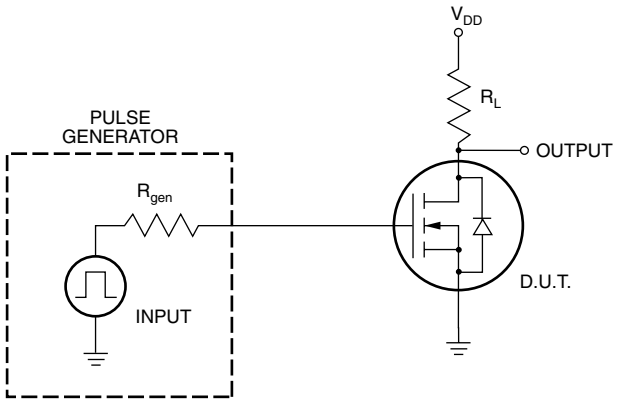
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60			V	V_{GS} = 0V, I_D = 100μA
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.5	V	V_{GS} = V_{DS}, I_D = 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-3.8		mV/°C	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage			100	nA	V_{GS} = 15V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	V_{GS} = 0V, V_{DS} = 45V
				500	μA	V_{GS} = 0V, V_{DS} = 45V, T_A 125°C
$I_{D(ON)}$	ON-State Drain Current	0.75			A	V_{GS} = 10V, V_{DS} = 10V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			7.5	Ω	V_{GS} = 5V, I_D = 0.2A
				5.0	Ω	V_{GS} = 10V, I_D = 500mA
$\Delta R_{DS(th)}$	Change in $R_{DS(th)}$ with Temperature		0.7		%/°C	V_{GS} = 10V, I_D = 500mA,
G_{FS}	Forward Transconductance	100			m℧	V_{DS} = 10V, I_D = 500mA
C_{ISS}	Input Capacitance		48	60	pF	V_{DS} = 25V, V_{GS} = 0V f = 1 MHz
C_{OSS}	Common Source Output Capacitance		16	25		
C_{RSS}	Reverse Transfer Capacitance		2	5		
$t_{(ON)}$	Turn-ON Time			10	ns	V_{DD} = 15V, I_D = 0.6A, R_{GEN} = 25Ω
$t_{(OFF)}$	Turn-OFF Time			10		
V_{SD}	Diode Forward Voltage Drop		0.8		V	V_{GS} = 0V, I_{SD} = 0.5A
t_{rr}	Reverse Recovery Time		160		ns	V_{GS} = 0V, I_{SD} = 0.5A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

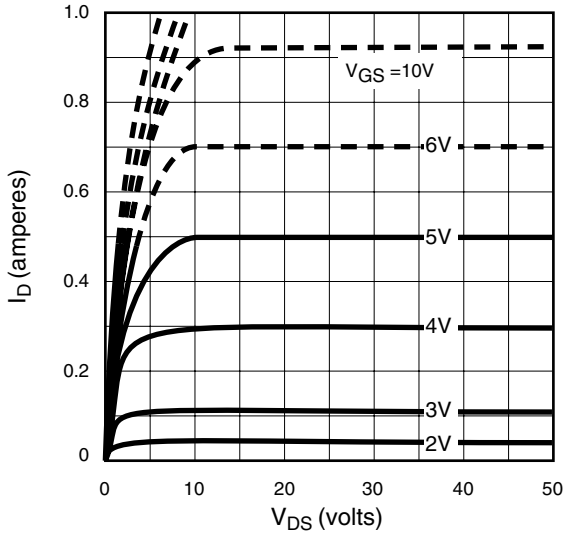
Switching Waveforms and Test Circuit



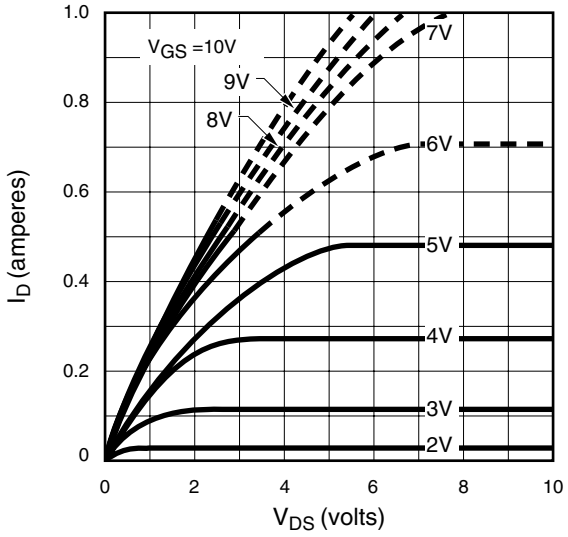


Typical Performance Curves

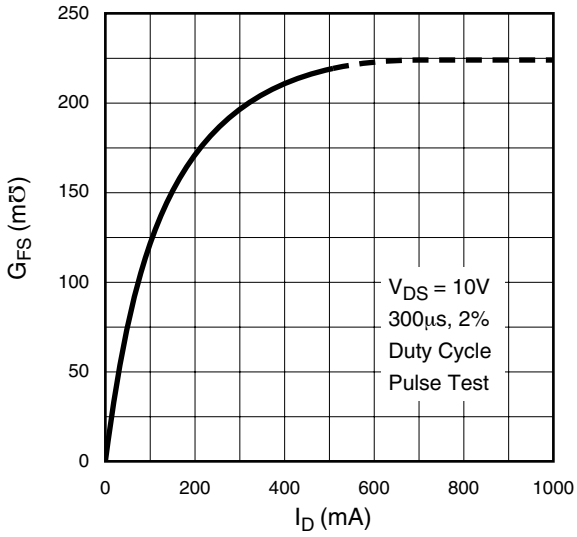
Output Characteristics



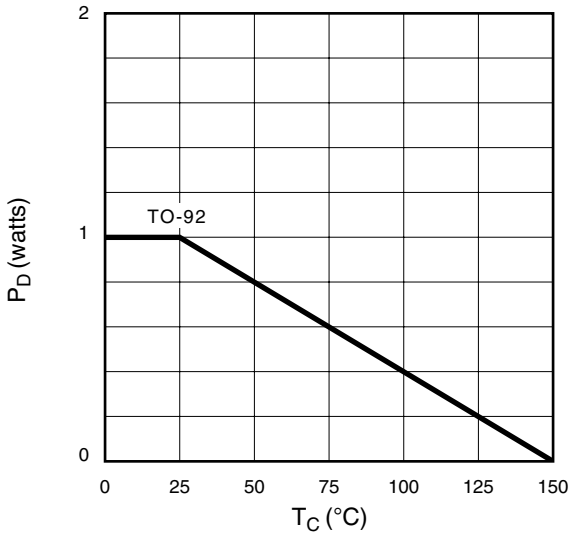
Saturation Characteristics



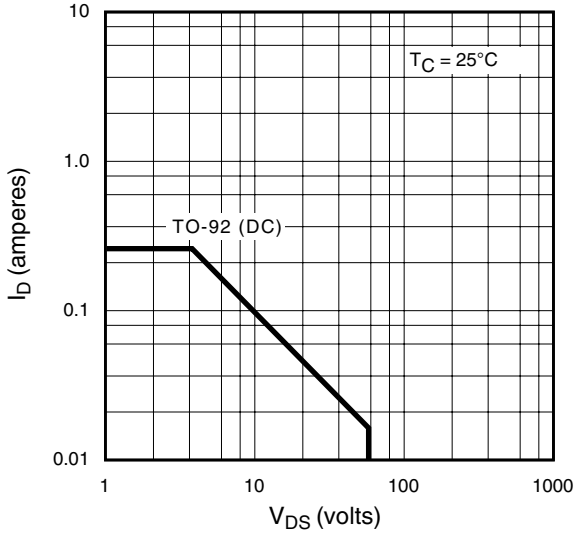
Transconductance vs. Drain Current



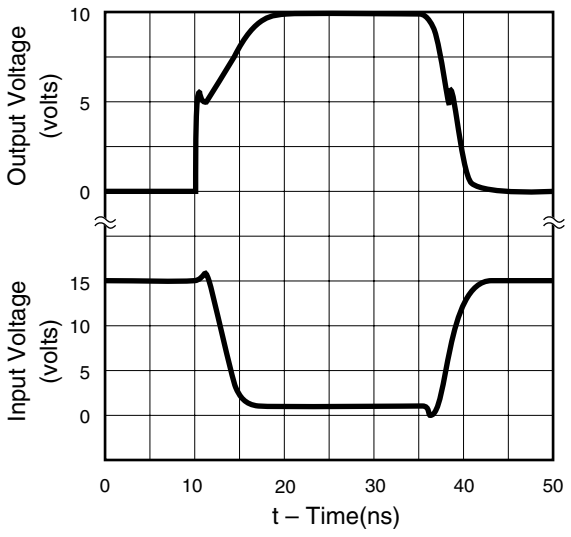
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

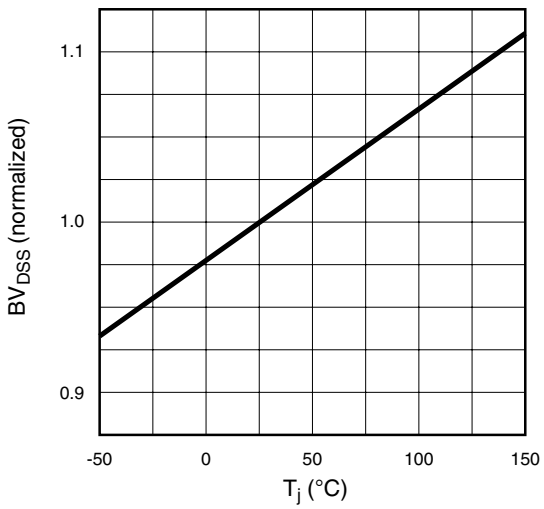


Switching Waveform

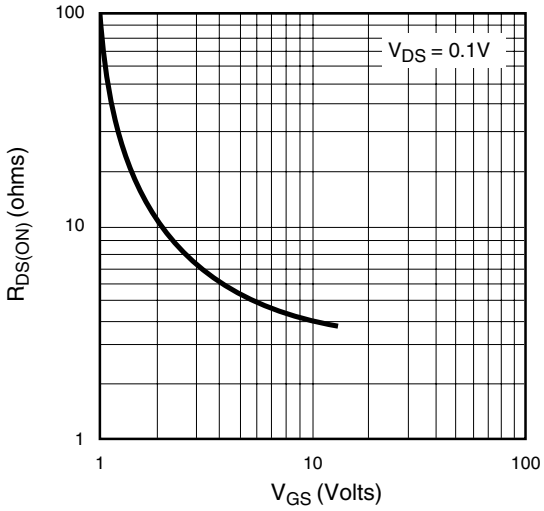


Typical Performance Curves

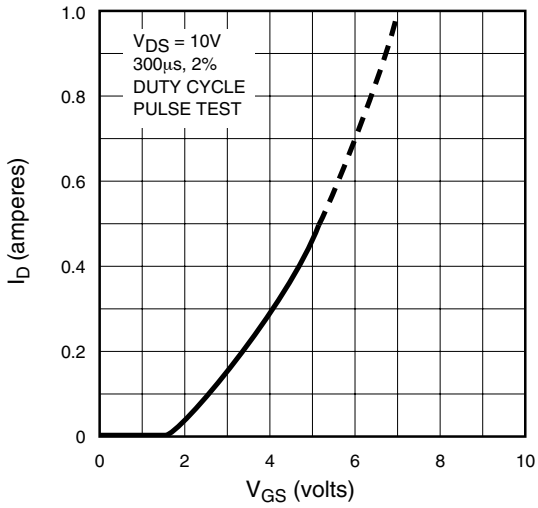
BV$_{DSS}$ Variation with Temperature



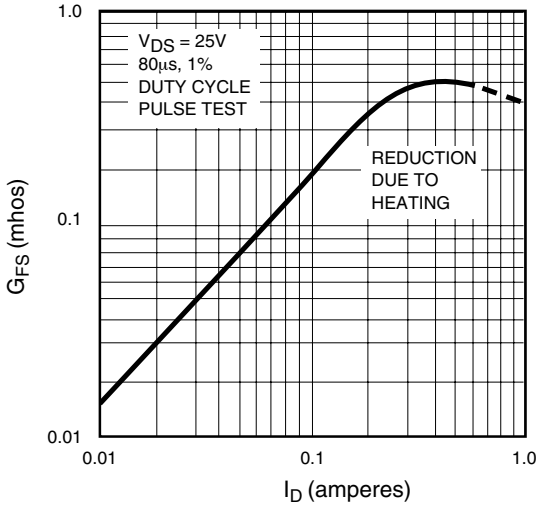
On-Resistance vs. Gate-to-Source Voltage



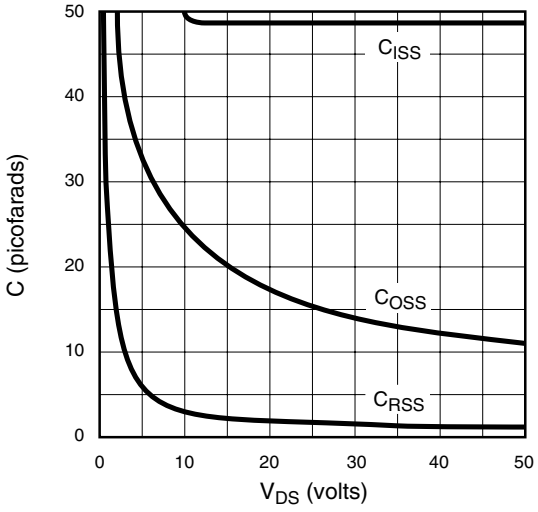
Transfer Characteristics



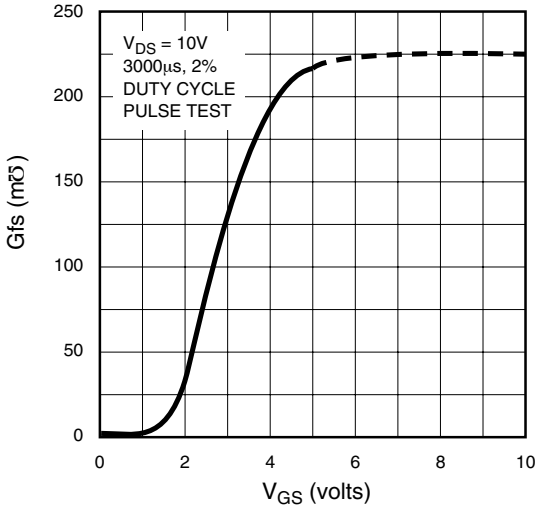
Output Conductance vs Drain Current



Capacitance vs. Drain-to-Source Voltage



Transconductance vs Gate-Source Voltage



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