# 100-MHz LOW-NOISE HIGH-SPEED AMPLIFIERS

## FEATURES

- **Ultralow 1.6 nV/√Hz Voltage Noise**
- **High Speed:**
  - **100-MHz Bandwidth [G = 2 (-1), –3 dB]**
  - **100-V/μs Slew Rate**
- **Very Low Distortion**
  - **THD = –72 dBc (f = 1 MHz, $R_L$ = 150 Ω)**
  - **THD = –90 dBc (f = 1 MHz, $R_L$ = 1 kΩ)**
- **Low 0.5-mV (Typ) Input Offset Voltage**
- **90-mA Output Current Drive (Typical)**
- **±5 V to ±15 V Typical Operation**
- **Available in Standard SOIC, MSOP PowerPAD™, JG, or FK Package**
- **Evaluation Module Available**

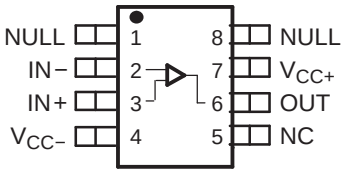
## DESCRIPTION

The THS4031 and THS4032 are ultralow-voltage noise, high-speed voltage feedback amplifiers that are ideal for applications requiring low voltage noise, including communications and imaging. The single amplifier THS4031 and the dual amplifier THS4032 offer very good ac performance with 100-MHz bandwidth (G = 2), 100-V/μs slew rate, and 60-ns settling time (0.1%). The THS4031 and THS4032 are unity gain stable with 275-MHz bandwidth. These amplifiers have a high drive capability of 90 mA and draw only 8.5-mA supply current per channel. With –90 dBc of total harmonic distortion (THD) at f = 1 MHz and a very low noise of 1.6 nV/√Hz, the THS4031 and THS4032 are ideally suited for applications requiring low distortion and low noise such as buffering analog-to-digital converters.

### RELATED DEVICES

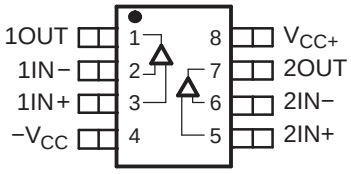
| DEVICE | DESCRIPTION |
|---|---|
| THS4051/2 | 70-MHz High-Speed Amplifiers |
| THS4081/2 | 175-MHz Low Power High-Speed Amplifiers |

**THS4031**
**D, DGN, AND JG PACKAGE**
**(TOP VIEW)**



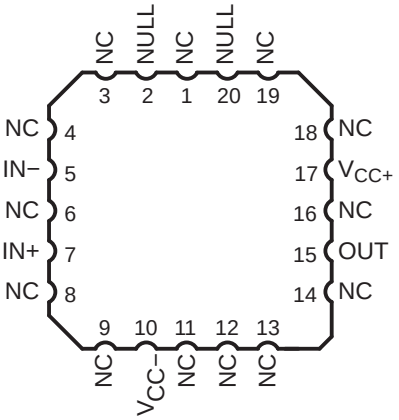

NC – No internal connection

**THS4032**
**D AND DGN PACKAGE**
**(TOP VIEW)**




Cross-Section View Showing PowerPAD™ Option (DGN)

**THS4031**
**FK PACKAGE**
**(TOP VIEW)**

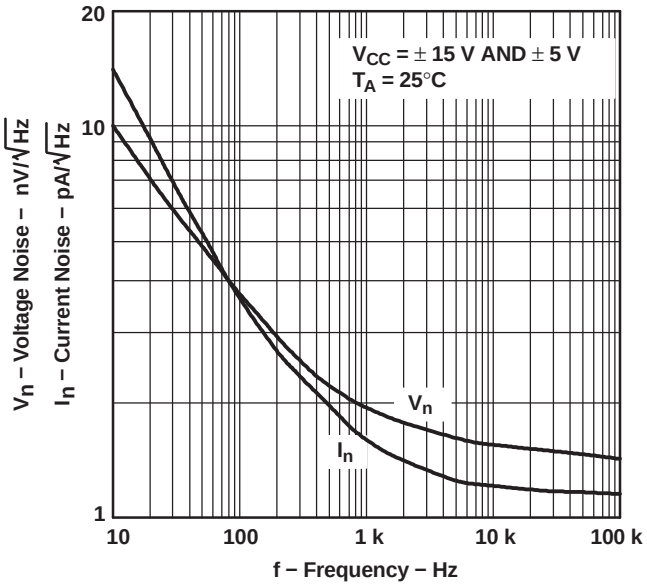



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**VOLTAGE NOISE AND CURRENT NOISE vs FREQUENCY**




## AVAILABLE OPTIONS[1]

| $T_A$ | NUMBER OF CHANNELS | PACKAGED DEVICES | | | | | EVALUATION MODULE |
|---|---|---|---|---|---|---|---|
| | | PLASTIC SMALL OUTLINE[2] (D) | PLASTIC MSOP[2](DGN)[3] | | CERAMIC DIP (JG) | CHIP CARRIER (FK) | |
| | | | DEVICE | SYMBOL | | | |
| 0°C to 70°C | 1 | THS4031CD | THS4031CDGN | TIACM | — | — | THS4031EVM |
| | 2 | THS4032CD | THS4032CDGN | TIABD | — | — | THS4032EVM |
| –40°C to 85°C | 1 | THS4031ID | THS4031IDGN | TIACN | — | — | — |
| | 2 | THS4032ID | THS4032IDGN | TIABG | — | — | — |
| –55°C to 125°C | 1 | — | — | — | THS4031MJG | THS4031MFK | — |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) The D and DGN packages are available taped and reeled. Add an R suffix to the device type (that is, THS4031CDGNR).
(3) The PowerPAD™ on the underside of the DGN package is electrically isolated from all other pins and active circuitry. Connection to the PCB ground plane is recommended, although not required, as this copper plane is typically the largest copper plane on the PCB.

## FUNCTIONAL BLOCK DIAGRAMS

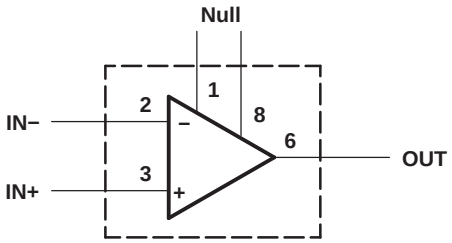



Figure 1. THS4031 – Single Channel

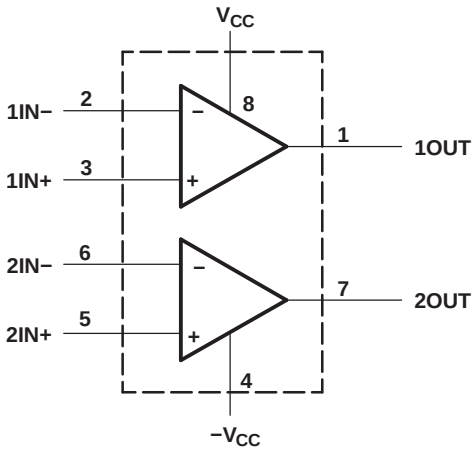



Figure 2. THS4032 – Dual Channel

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage, $V_{CC+}$ to $V_{CC-}$ | | 33 | V |
| $V_I$ | Input voltage | | $\pm V_{CC}$ | |
| $I_O$ | Output current | | 150 | mA |
| $V_{IO}$ | Differential input voltage | | ±4 | V |
| | Continuous total power dissipation | | See Dissipation Ratings Table | |
| $T_A$ | Operating free-air temperature | C-suffix | 0 to 70 | °C |
| | | I-suffix | –40 to 85 | |
| | | M-suffix | –55 to 125 | |
| $T_J$ | Maximum junction temperature, (any condition) | | 150 | °C |
| | Maximum junction temperature, continuous operation, long term reliability(2) | | 130 | °C |
| $T_{stg}$ | Storage temperature | | –65 to 150 | °C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | 300 | °C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, JG package | | 300 | °C |
| | Case temperature for 60 seconds, FK package | | 260 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device. Does not apply to the JG package or FK package.

## DISSIPATION RATINGS TABLE

| PACKAGE | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) | $T_A$ = 25°C, POWER RATING |
|---|---|---|---|
| D | 167(1) | 38.3 | 629 mW, $T_J$ = 130°C, continuous |
| DGN(2) | 58.4 | 4.7 | 1.8 W, $T_J$ = 130°C, continuous |
| JG | 119 | 28 | 1050 mW, $T_J$ = 150°C, continuous |
| FK | 87.7 | 20 | 1375 mW, $T_J$ = 150°C, continuous |

(1) This data was taken using the JEDEC standard Low-K test PCB. For the JEDEC Proposed High-K test PCB, the $\theta_{JA}$ is 95°C/W with a power rating at $T_A$ = 25°C of 1.32 W.
(2) This data was taken using 2 oz. trace and copper pad that is soldered directly to a 3-in. × 3-in. PC. For further information, refer to *Application Information* section of this data sheet.

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC+}$ and $V_{CC-}$ | Supply voltage | Dual supply | ±4.5 | | ±16 | V |
| | | Single supply | 9 | | 32 | |
| $T_A$ | Operating free-air temperature | C-suffix | 0 | | 70 | °C |
| | | I-suffix | –40 | | 85 | |
| | | M-suffix | –55 | | 125 | |

## ELECTRICAL CHARACTERISTICS

At $T_A$ = 25°C, $V_{CC}$ = ±15 V, and $R_L$ = 150 Ω (unless otherwise noted).

| PARAMETER | | | TEST CONDITIONS[1] | | | THS403xC, THS403xI MIN | THS403xC, THS403xI TYP | THS403xC, THS403xI MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **DYNAMIC PERFORMANCE** | | | | | | | | | |
| BW | Small-signal bandwidth (–3 dB) | | $V_{CC}$ = ±15 V | | Gain = –1 or 2 | | 100 | | MHz |
| | | | $V_{CC}$ = ±5 V | | | | 90 | | |
| | Bandwidth for 0.1-dB flatness | | $V_{CC}$ = ±15 V | | Gain = –1 or 2 | | 50 | | MHz |
| | | | $V_{CC}$ = ±5 V | | | | 45 | | |
| | Full power bandwidth[2] | | $V_{O(pp)}$ = 20 V, | $V_{CC}$ = ±15 V | $R_L$ = 1 kΩ | | 2.3 | | MHz |
| | | | $V_{O(pp)}$ = 5 V, | $V_{CC}$ = ±5 V | | | 7.2 | | |
| SR | Slew rate[3] | | $V_{CC}$ = ±15 V, | 20-V step | Gain = –1 | | 100 | | V/µs |
| | | | $V_{CC}$ = ±5 V, | 5-V step | | | 80 | | |
| $t_S$ | Settling time to 0.1% | | $V_{CC}$ = ±15 V, | 5-V step | Gain = –1 | | 60 | | ns |
| | | | $V_{CC}$ = ±5 V, | 2.5-V step | | | 45 | | |
| | Settling time to 0.01% | | $V_{CC}$ = ±15 V, | 5-V step | Gain = –1 | | 90 | | ns |
| | | | $V_{CC}$ = ±5 V, | 2.5-V step | | | 80 | | |
| **NOISE/DISTORTION PERFORMANCE** | | | | | | | | | |
| THD | Total harmonic distortion | THS4031 | $V_{CC}$ = ±5 V or ±15 V, f = 1 MHz | $V_{O(pp)}$ = 2 V, Gain = 2 | $R_L$ = 150 Ω | | –81 | | dBc |
| | | | | | $R_L$ = 1 kΩ | | –96 | | |
| | | THS4032 | | | $R_L$ = 150 Ω | | –72 | | |
| | | | | | $R_L$ = 1 kΩ | | –90 | | |
| $V_n$ | Input voltage noise | | $V_{CC}$ = ±5 V or ±15 V, | f > 10 kHz | | | 1.6 | | nA/√Hz |
| $I_n$ | Input current noise | | $V_{CC}$ = ±5 V or ±15 V, | f > 10 kHz | | | 1.2 | | pA/√Hz |
| | Differential gain error | | Gain = 2, 40 IRE modulation, | NTSC and PAL, ±100 IRE ramp | $V_{CC}$ = ±15 V | | 0.015% | | |
| | | | | | $V_{CC}$ = ±5 V | | 0.02% | | |
| | Differential phase error | | | | $V_{CC}$ = ±15 V | | 0.025 | | ° |
| | | | | | $V_{CC}$ = ±5 V | | 0.03 | | |
| | Channel-to-channel crosstalk (THS4032 only) | | $V_{CC}$ = ±5 V or ±15 V, | f = 1 MHz | | | –61 | | dBc |

(1) Full range = 0°C to 70°C for THS403xC and –40°C to 85°C for THS403xI suffix.
(2) Full power bandwidth = slew rate / [$\sqrt{2}\,\pi V_{OC(Peak)}$].
(3) Slew rate is measured from an output level range of 25% to 75%.

## ELECTRICAL CHARACTERISTICS (continued)

At $T_A$ = 25°C, $V_{CC}$ = ±15 V, and $R_L$ = 150 Ω (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS[1] | | THS403xC, THS403xI | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| **DC PERFORMANCE** | | | | | | | |
| | Open loop gain | $V_{CC}$ = ±15 V, $R_L$ = 1 kΩ, $V_O$ = ±10 V | $T_A$ = 25°C | 93 | 98 | | dB |
| | | | $T_A$ = full range | 92 | | | |
| | | $V_{CC}$ = ±5 V, $R_L$ = 1 kΩ, $V_O$ = ±2.5 V | $T_A$ = 25°C | 90 | 95 | | |
| | | | $T_A$ = full range | 89 | | | |
| $V_{OS}$ | Input offset voltage | $V_{CC}$ = ±5 V or ±15 V | $T_A$ = 25°C | | 0.5 | 2 | mV |
| | | | $T_A$ = full range | | | 3 | |
| $I_{IB}$ | Input bias current | $V_{CC}$ = ±5 V or ±15 V | $T_A$ = 25°C | | 3 | 6 | µA |
| | | | $T_A$ = full range | | | 8 | |
| $I_{OS}$ | Input offset current | $V_{CC}$ = ±5 V or ±15 V | $T_A$ = 25°C | | 30 | 250 | nA |
| | | | $T_A$ = full range | | | 400 | |
| | Offset voltage drift | $V_{CC}$ = ±5 V or ±15 V | $T_A$ = full range | | 2 | | µV/°C |
| | Input offset current drift | $V_{CC}$ = ±5 V or ±15 V | $T_A$ = full range | | 0.2 | | nA/°C |
| **INPUT CHARACTERISTICS** | | | | | | | |
| $V_{ICR}$ | Common-mode input voltage range | $V_{CC}$ = ±15 V | | ±13.5 | ±14.0 | | V |
| | | $V_{CC}$ = ±5 V | | ±3.8 | ±4.0 | | |
| CMRR | Common-mode rejection ratio | $V_{CC}$ = ±15 V, $V_{ICR}$ = ±12 V | $T_A$ = 25°C | 85 | 95 | | dB |
| | | | $T_A$ = full range | 80 | | | |
| | | $V_{CC}$ = ±5 V, $V_{ICR}$ = ±2.5 V | $T_A$ = 25°C | 90 | 100 | | |
| | | | $T_A$ = full range | 85 | | | |
| $r_i$ | Input resistance | | | | 2 | | MΩ |
| $C_i$ | Input capacitance | | | | 1.5 | | pF |
| **OUTPUT CHARACTERISTICS** | | | | | | | |
| $V_O$ | Output voltage swing | $V_{CC}$ = ±15 V | $R_L$ = 1 kΩ | ±13 | ±13.6 | | V |
| | | $V_{CC}$ = ±5 V | | ±3.4 | ±3.8 | | |
| | | $V_{CC}$ = ±15 V | $R_L$ = 150 Ω | ±12 | ±12.9 | | |
| | | $V_{CC}$ = ±5 V | $R_L$ = 250 Ω | ±3 | ±3.5 | | |
| $I_O$ | Output current[4] | $V_{CC}$ = ±15 V | $R_L$ = 20 Ω | 60 | 90 | | mA |
| | | $V_{CC}$ = ±5 V | | 50 | 70 | | |
| $I_{SC}$ | Short-circuit current[4] | $V_{CC}$ = ±15 V | | | 150 | | mA |
| $R_O$ | Output resistance | Open loop | | | 13 | | Ω |
| **POWER SUPPLY** | | | | | | | |
| $V_{CC}$ | Supply voltage operating range | Dual supply | | ±4.5 | | ±16.5 | V |
| | | Single supply | | 9 | | 33 | |
| $I_{CC}$ | Supply current (each amplifier) | $V_{CC}$ = ±15 V | $T_A$ = 25°C | | 8.5 | 10 | mA |
| | | | $T_A$ = full range | | | 11 | |
| | | $V_{CC}$ = ±5 V | $T_A$ = 25°C | | 7.5 | 9 | |
| | | | $T_A$ = full range | | | 10.5 | |
| PSRR | Power-supply rejection ratio | $V_{CC}$ = ±5 V or ±15 V | $T_A$ = 25°C | 85 | 95 | | dB |
| | | | $T_A$ = full range | 80 | | | |

(4) Observe power dissipation ratings to keep the junction temperature below the absolute maximum rating when the output is heavily loaded or shorted. See the Absolute Maximum Ratings table in this data sheet for more information.

## ELECTRICAL CHARACTERISTICS

At $T_A$ = full range, $V_{CC}$ = ±15 V, and $R_L$ = 1 kΩ (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS[1] | | | THS403xC, THS403xI | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| **DYNAMIC PERFORMANCE** | | | | | | | | |
| BW | Unity gain bandwidth | $V_{CC}$ = ±15 V, | Closed loop | $R_L$ = 1 kΩ | 100[2] | 120 | | MHz |
| | Small-signal bandwidth (–3 dB) | $V_{CC}$ = ±15 V | | Gain = –1 or 2 | | 100 | | MHz |
| | | $V_{CC}$ = ±5 V | | | | 90 | | |
| | Bandwidth for 0.1-dB flatness | $V_{CC}$ = ±15 V | | Gain = –1 or 2 | | 50 | | MHz |
| | | $V_{CC}$ = ±5 V | | | | 45 | | |
| | Full power bandwidth[3] | $V_{O(pp)}$ = 20 V, | $V_{CC}$ = ±15 V | $R_L$ = 1 kΩ | | 2.3 | | MHz |
| | | $V_{O(pp)}$ = 5 V, | $V_{CC}$ = ±5 V | | | 7.1 | | |
| SR | Slew rate | $V_{CC}$ = ±15 V | | $R_L$ = 1 kΩ | 80[2] | 100 | | V/µs |
| $t_S$ | Settling time to 0.1% | $V_{CC}$ = ±15 V, | 5-V step | Gain = –1 | | 60 | | ns |
| | | $V_{CC}$ = ±5 V, | 2.5-V step | | | 45 | | |
| | Settling time to 0.01% | $V_{CC}$ = ±15 V, | 5-V step | Gain = –1 | | 90 | | ns |
| | | $V_{CC}$ = ±5 V, | 2.5-V step | | | 80 | | |
| **NOISE/DISTORTION PERFORMANCE** | | | | | | | | |
| THD | Total harmonic distortion | $V_{CC}$ = ±5 V or ±15 V, f = 1 MHz, Gain = 2, | $V_{O(pp)}$ = 2 V, $T_A$ = 25°C | $R_L$ = 150 Ω | | –81 | | dBc |
| | | | | $R_L$ = 1 kΩ | | –96 | | |
| $V_n$ | Input voltage noise | $V_{CC}$ = ±5 V or ±15 V, $T_A$ = 25°C | f > 10 kHz | $R_L$ = 150 Ω | | 1.6 | | nA/√Hz |
| $I_n$ | Input current noise | $V_{CC}$ = ±5 V or ±15 V, $T_A$ = 25°C | f > 10 kHz | $R_L$ = 150 Ω | | 1.2 | | pA/√Hz |
| | Differential gain error | Gain = 2, 40 IRE modulation, $T_A$ = 25°C | NTSC and PAL, ±100 IRE ramp, $R_L$ = 150 Ω | $V_{CC}$ = ±15 V | | 0.015% | | |
| | | | | $V_{CC}$ = ±5 V | | 0.02% | | |
| | Differential phase error | | | $V_{CC}$ = ±15 V | | 0.025 | | ° |
| | | | | $V_{CC}$ = ±5 V | | 0.03 | | |
| **DC PERFORMANCE** | | | | | | | | |
| | Open loop gain | $V_{CC}$ = ±15 V, $R_L$ = 1 kΩ, $V_O$ = ±10 V | | $T_A$ = 25°C | 93 | 98 | | dB |
| | | | | $T_A$ = full range | 92 | | | |
| | | $V_{CC}$ = ±5 V, $R_L$ = 1 kΩ, $V_O$ = ±2.5 V | | $T_A$ = 25°C | 92 | 95 | | |
| | | | | $T_A$ = full range | 91 | | | |
| $V_{OS}$ | Input offset voltage | $V_{CC}$ = ±5 V or ±15 V | | $T_A$ = 25°C | | 0.5 | 2 | mV |
| | | | | $T_A$ = full range | | | 3 | |
| $I_{IB}$ | Input bias current | $V_{CC}$ = ±5 V or ±15 V | | $T_A$ = 25°C | | 3 | 6 | µA |
| | | | | $T_A$ = full range | | | 8 | |
| $I_{OS}$ | Input offset current | $V_{CC}$ = ±5 V or ±15 V | | $T_A$ = 25°C | | 30 | 250 | nA |
| | | | | $T_A$ = full range | | | 400 | |
| | Offset voltage drift | $V_{CC}$ = ±5 V or ±15 V | | $T_A$ = full range | | 2 | | µV/°C |
| | Input offset current drift | $V_{CC}$ = ±5 V or ±15 V | | $T_A$ = full range | | 0.2 | | nA/°C |

(1) Full range = 0°C to 70°C for THS403xC and –40°C to 85°C for THS403xI suffix.
(2) This parameter is not tested.
(3) Full power bandwidth = slew rate / $[\sqrt{2}\,\pi V_{OC(Peak)}]$.

## ELECTRICAL CHARACTERISTICS (continued)

At $T_A$ = full range, $V_{CC}$ = ±15 V, and $R_L$ = 1 kΩ (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS[1] | | THS403xC, THS403xI | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| **INPUT CHARACTERISTICS** | | | | | | | |
| $V_{ICR}$ | Common-mode input voltage range | $V_{CC}$ = ±15 V | | ±13.5 | ±14.3 | | V |
| | | $V_{CC}$ = ±5 V | | ±3.8 | ±4.3 | | |
| CMRR | Common-mode rejection ratio | $V_{CC}$ = ±15 V, $V_{ICR}$ = ±12 V | $T_A$ = 25°C | 85 | 95 | | dB |
| | | | $T_A$ = full range | 80 | | | |
| | | $V_{CC}$ = ±5 V, $V_{ICR}$ = ±2.5 V | $T_A$ = 25°C | 90 | 100 | | |
| | | | $T_A$ = full range | 85 | | | |
| $r_i$ | Input resistance | | | | 2 | | MΩ |
| $C_i$ | Input capacitance | | | | 1.5 | | pF |
| **OUTPUT CHARACTERISTICS** | | | | | | | |
| $V_O$ | Output voltage swing | $V_{CC}$ = ±15 V | $R_L$ = 1 kΩ | ±13 | ±13.6 | | V |
| | | $V_{CC}$ = ±5 V | | ±3.4 | ±3.8 | | |
| | | $V_{CC}$ = ±15 V | $R_L$ = 150 Ω | ±12 | ±12.9 | | |
| | | $V_{CC}$ = ±5 V | $R_L$ = 250 Ω | ±3 | ±3.5 | | |
| $I_O$ | Output current[4] | $V_{CC}$ = ±15 V | $R_L$ = 20 Ω | 60 | 90 | | mA |
| | | $V_{CC}$ = ±5 V | | 50 | 70 | | |
| $I_{SC}$ | Short-circuit current[4] | $V_{CC}$ = ±15 V | | | 150 | | mA |
| $R_O$ | Output resistance | Open loop | | | 13 | | Ω |
| **POWER SUPPLY** | | | | | | | |
| $V_{CC}$ | Supply voltage operating range | Dual supply | | ±4.5 | | ±16.5 | V |
| | | Single supply | | 9 | | 33 | |
| $I_{CC}$ | Supply current (each amplifier) | $V_{CC}$ = ±15 V | $T_A$ = 25°C | | 8.5 | 10 | mA |
| | | | $T_A$ = full range | | | 11 | |
| | | $V_{CC}$ = ±5 V | $T_A$ = 25°C | | 7.5 | 9 | |
| | | | $T_A$ = full range | | | 10 | |
| PSRR | Power-supply rejection ratio | $V_{CC}$ = ±5 V or ±15 V | $T_A$ = 25°C | 85 | 95 | | dB |
| | | | $T_A$ = full range | 80 | | | |

(4) Observe power dissipation ratings to keep the junction temperature below the absolute maximum rating when the output is heavily loaded or shorted. See the Absolute Maximum Ratings table in this data sheet for more information.

## PARAMETER MEASUREMENT INFORMATION

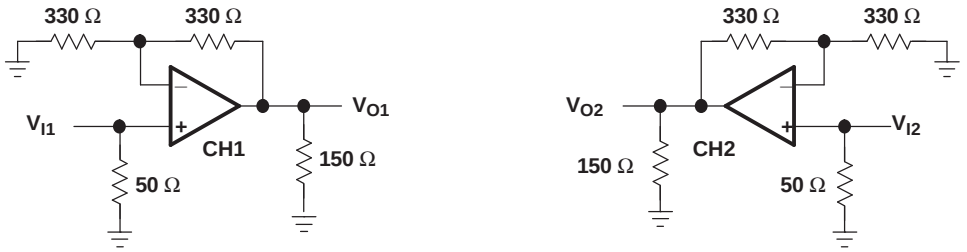



**Figure 3. THS4032 Crosstalk Test Circuit**

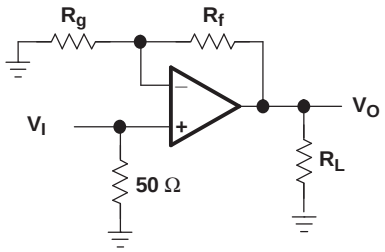



**Figure 4. Step Response Test Circuit**

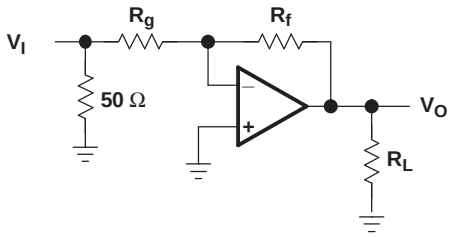



**Figure 5. Step Response Test Circuit**

## TYPICAL CHARACTERISTICS

### Table of Graphs

| | | FIGURE |
|---|---|---|
| Input offset voltage distribution | | 6, 7 |
| Input offset voltage | vs Free-air temperature | 8 |
| Input bias current | vs Free-air temperature | 9 |
| Output voltage swing | vs Supply voltage | 10 |
| Maximum output voltage swing | vs Free-air temperature | 11 |
| Maximum output current | vs Free-air temperature | 12 |
| Supply current | vs Free-air temperature | 13 |
| Common-mode input voltage | vs Supply voltage | 14 |
| Closed-loop output impedance | vs Frequency | 15 |
| Open-loop gain and phase response | vs Frequency | 16 |
| Power-supply rejection ratio | vs Frequency | 17 |
| Common-mode rejection ratio | vs Frequency | 18 |
| Crosstalk | vs Frequency | 19 |
| Harmonic distortion | vs Frequency | 20, 21 |
| Harmonic distortion | vs Peak-to-peak output voltage | 22, 23 |
| Slew rate | vs Free-air temperature | 24 |
| 0.1% settling time | vs Output voltage step size | 25 |
| Small signal frequency response with varying feedback resistance | Gain = 1, $V_{CC}$ = ±15V, $R_L$ = 1kΩ | 26 |
| Frequency response with varying output voltage swing | Gain = 1, $V_{CC}$ = ±15V, $R_L$ = 1kΩ | 27 |
| Small signal frequency response with varying feedback resistance | Gain = 1, $V_{CC}$ = ±15V, $R_L$ = 150kΩ | 28 |
| Frequency response with varying output voltage swing | Gain = 1, $V_{CC}$ = ±15V, $R_L$ = 150kΩ | 29 |
| Small signal frequency response with varying feedback resistance | Gain = 1, $V_{CC}$ = ±5V, $R_L$ = 1kΩ | 30 |
| Frequency response with varying output voltage swing | Gain = 1, $V_{CC}$ = ±5V, $R_L$ = 1kΩ | 31 |
| Small signal frequency response with varying feedback resistance | Gain = 1, $V_{CC}$ = ±5V, $R_L$ = 150kΩ | 32 |
| Frequency response with varying output voltage swing | Gain = 1, $V_{CC}$ = ±5V, $R_L$ = 150kΩ | 33 |
| Small signal frequency response with varying feedback resistance | Gain = 2, $V_{CC}$ = ±5V, $R_L$ = 150kΩ | 34 |
| Small signal frequency response with varying feedback resistance | Gain = 2, $V_{CC}$ = ±5V, $R_L$ = 150kΩ | 35 |
| Small signal frequency response with varying feedback resistance | Gain = –1, $V_{CC}$ = ±15V, $R_L$ = 150kΩ | 36 |
| Frequency response with varying output voltage swing | Gain = –1, $V_{CC}$ = ±5V, $R_L$ = 150kΩ | 37 |
| Small signal frequency response | Gain = 5, $V_{CC}$ = ±15V, ±5V | 38 |
| Output amplitude | vs Frequency, Gain = 2, $V_S$ = ±15V | 39 |
| Output amplitude | vs Frequency, Gain = 2, $V_S$ = ±5V | 40 |
| Output amplitude | vs Frequency, Gain = –1, $V_S$ = ±15V | 41 |
| Output amplitude | vs Frequency, Gain = –1, $V_S$ = ±5V | 42 |
| Differential phase | vs Number of 150Ω loads | 43, 44 |
| Differential gain | vs Number of 150Ω loads | 45, 46 |
| 1-V step response | vs Time | 47, 48 |
| 4-V step response | vs Time | 49 |
| 20-V step response | vs Time | 50 |

## TYPICAL CHARACTERISTICS

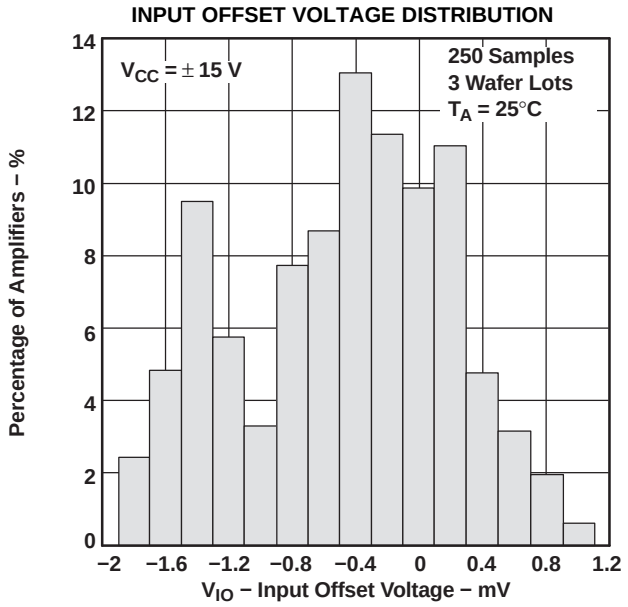



Figure 6.

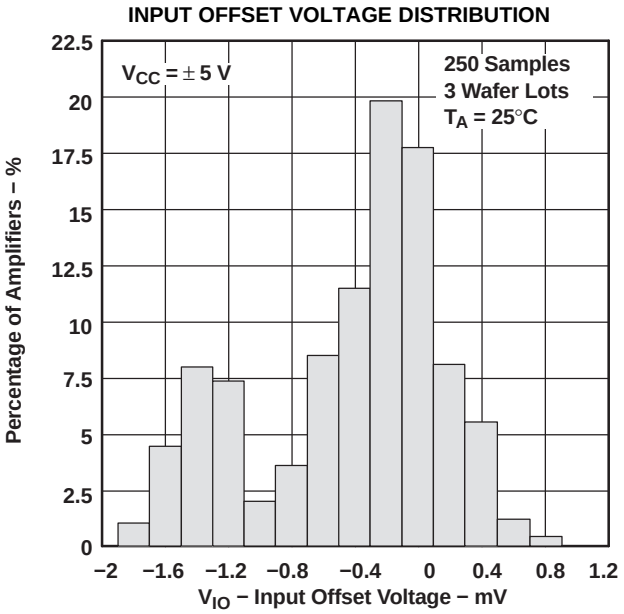



Figure 7.

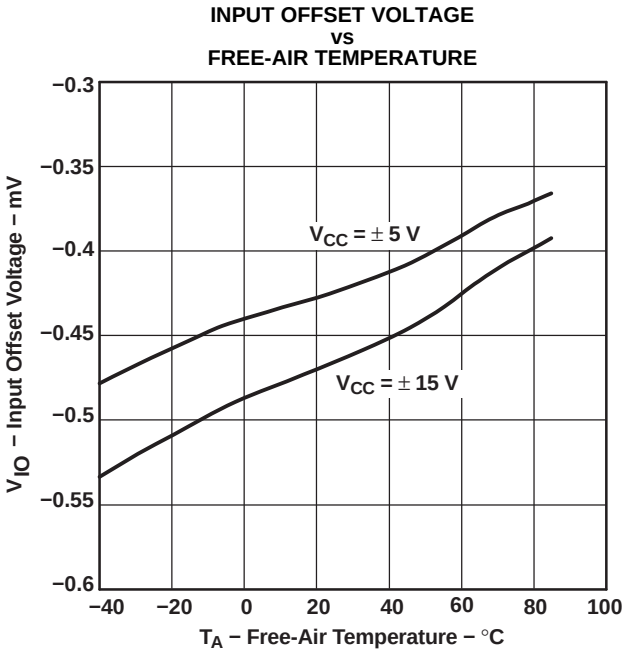



Figure 8.

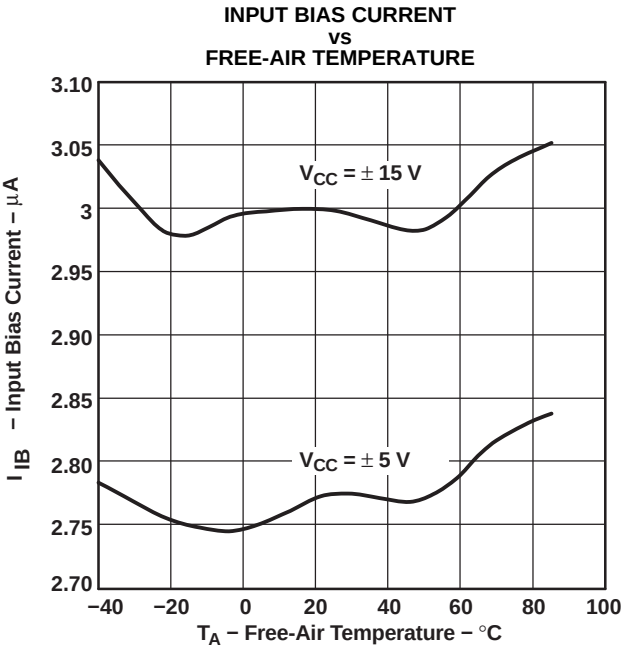



Figure 9.

## TYPICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE SWING
vs
SUPPLY VOLTAGE

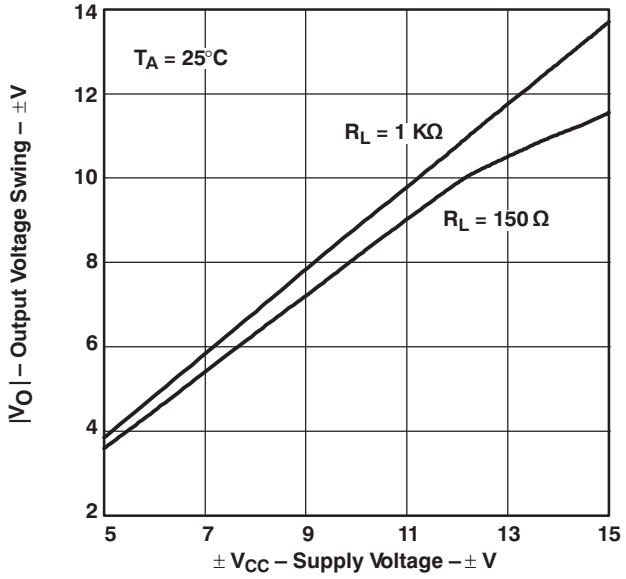



Figure 10.

MAXIMUM OUTPUT VOLTAGE SWING
vs
FREE-AIR TEMPERATURE

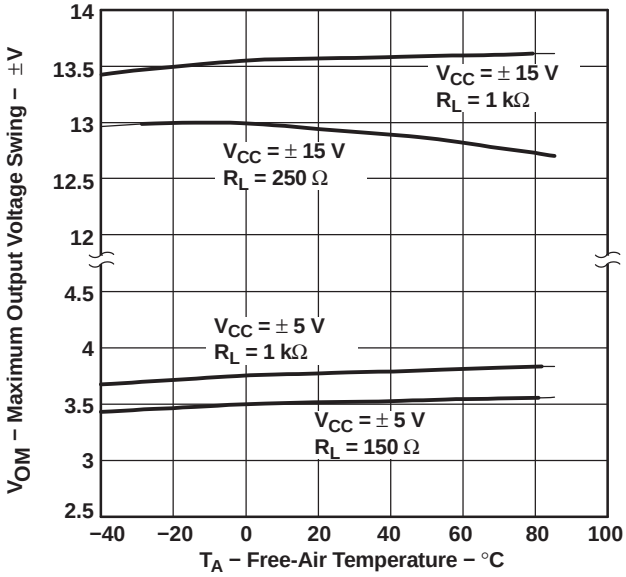



Figure 11.

MAXIMUM OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

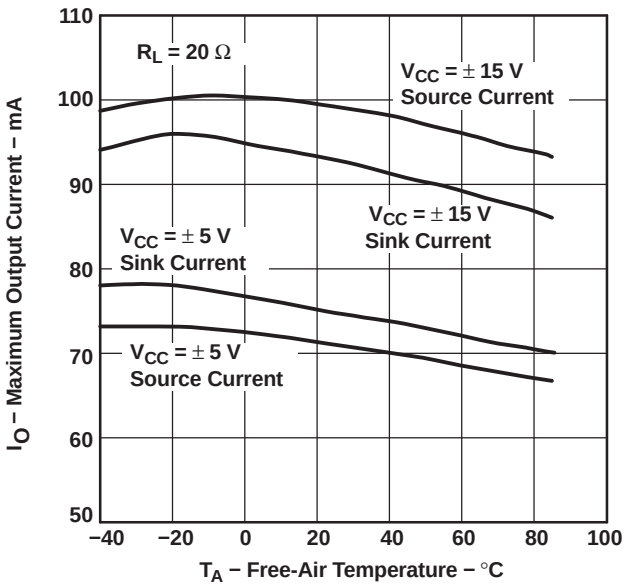



Figure 12.

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

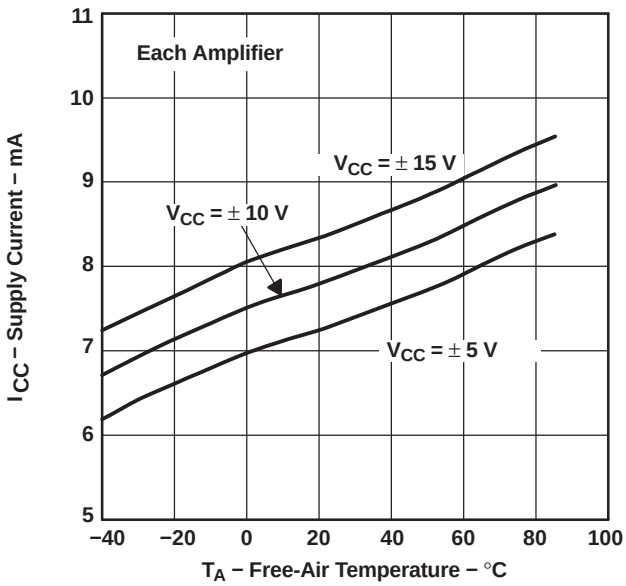



Figure 13.

## TYPICAL CHARACTERISTICS (continued)

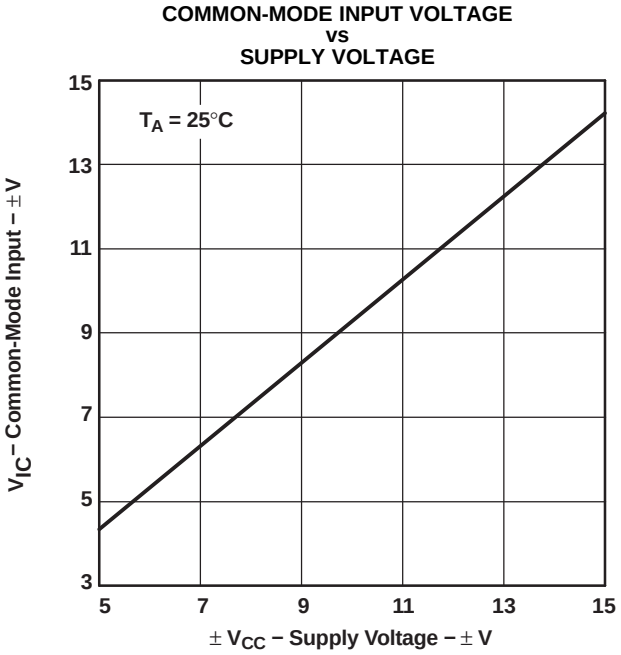



Figure 14.

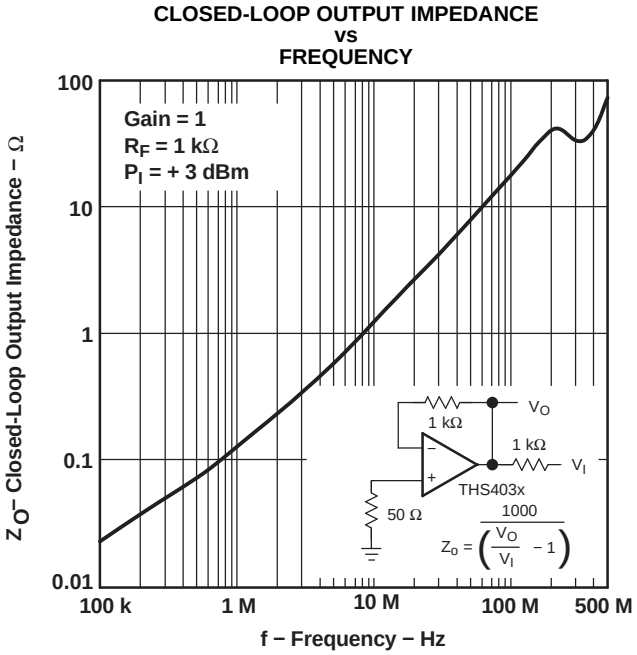



Figure 15.

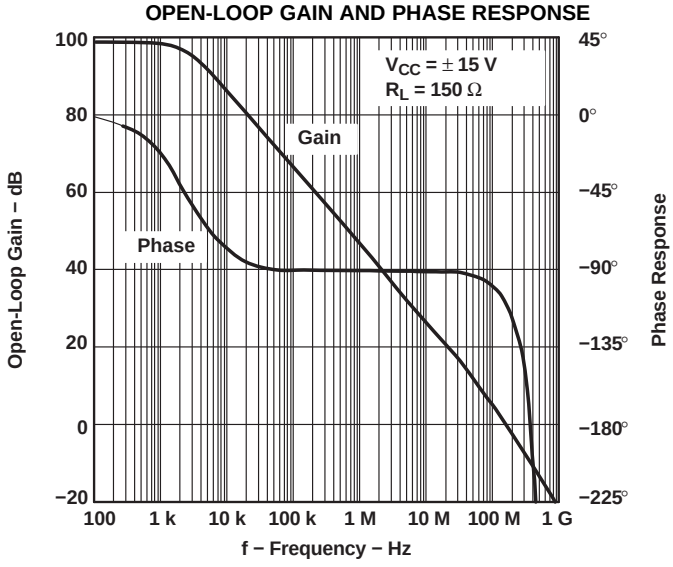



Figure 16.

## TYPICAL CHARACTERISTICS (continued)

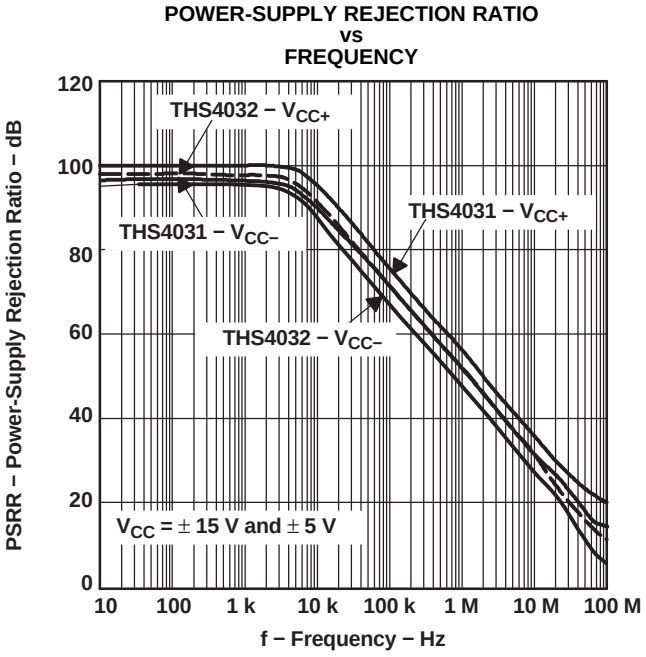



Figure 17.

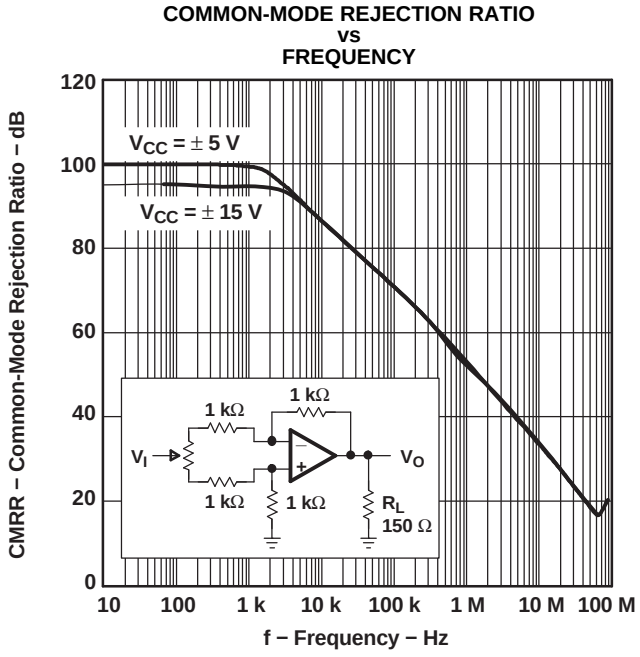



Figure 18.

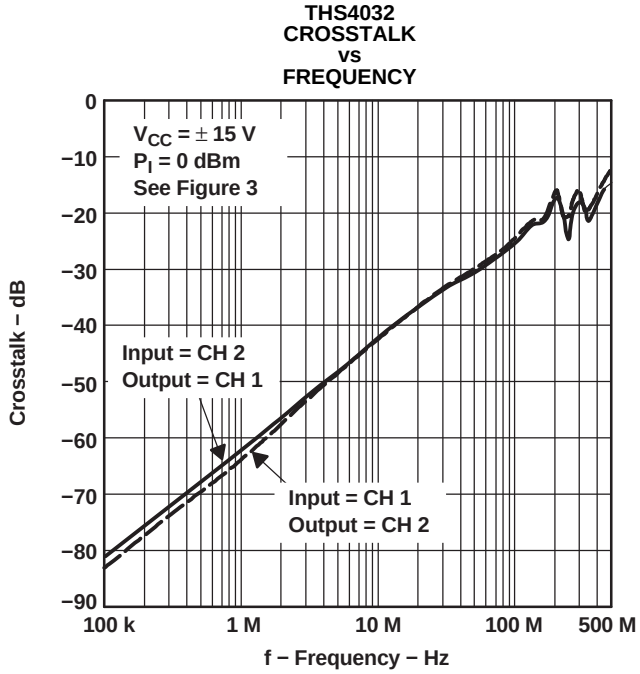



Figure 19.

## TYPICAL CHARACTERISTICS (continued)

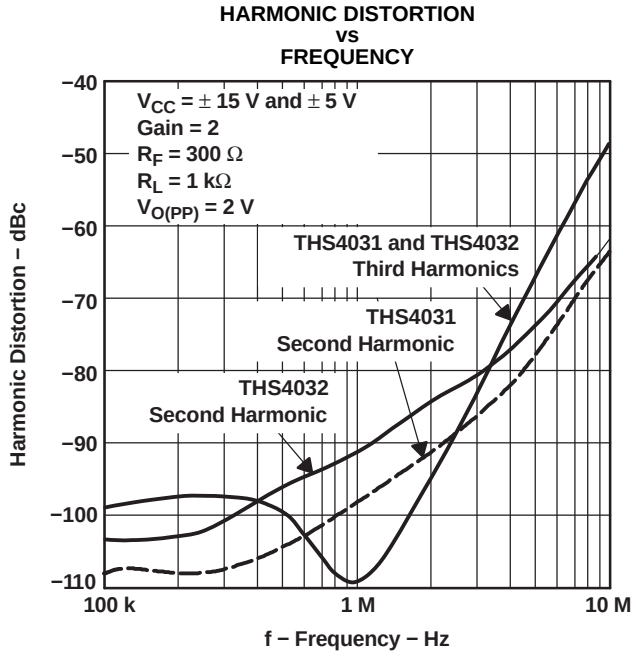



Figure 20.

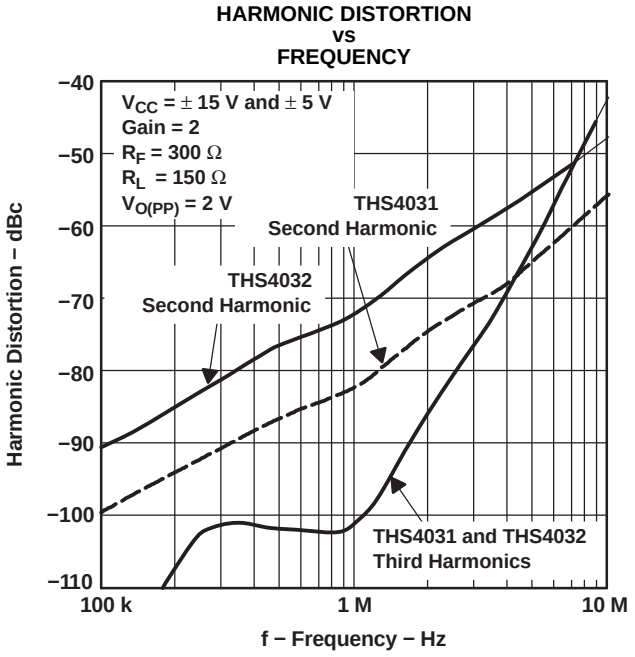



Figure 21.

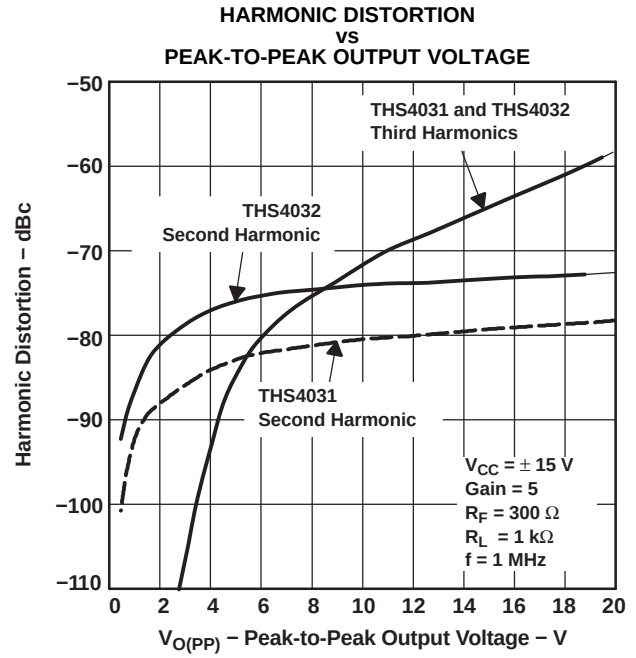



Figure 22.

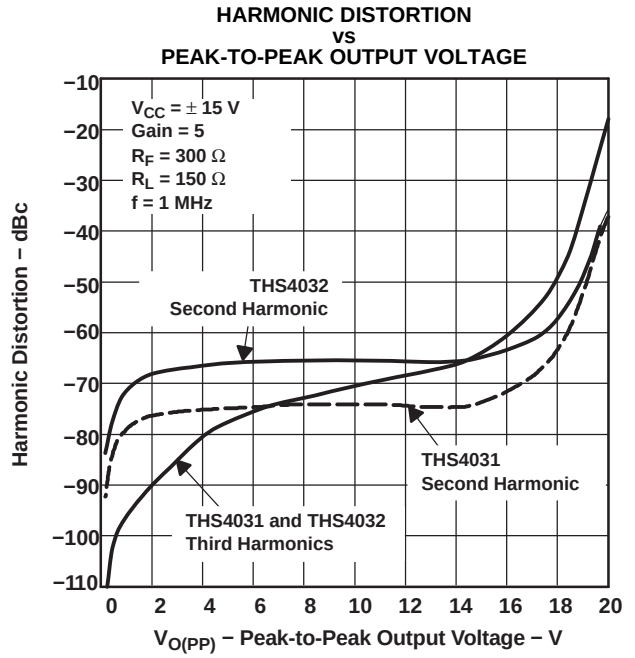



Figure 23.

## TYPICAL CHARACTERISTICS (continued)

**SLEW RATE vs FREE-AIR TEMPERATURE**

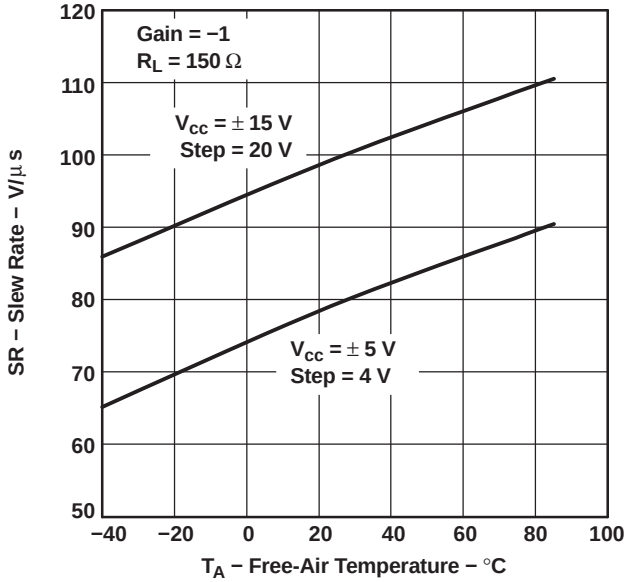



Figure 24.

**0.1% SETTLING TIME vs OUTPUT VOLTAGE STEP SIZE**

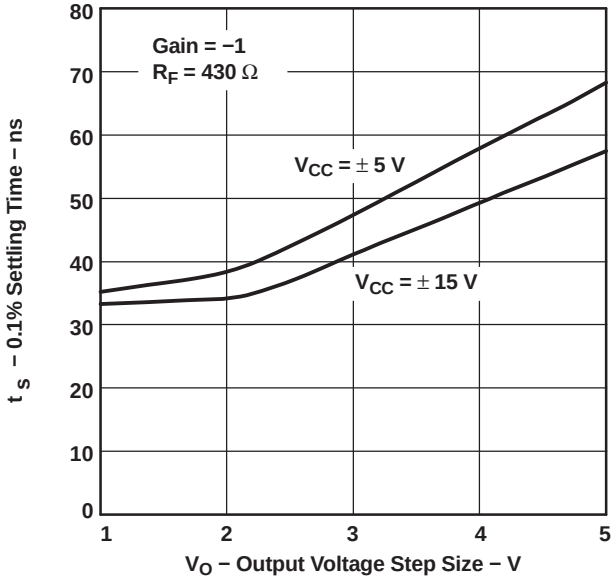



Figure 25.

**SMALL SIGNAL FREQUENCY RESPONSE WITH VARYING FEEDBACK RESISTANCE**

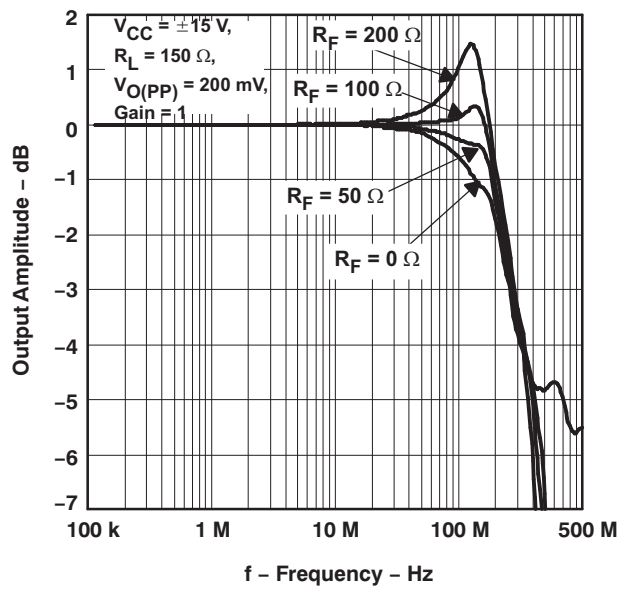



Figure 26.

**FREQUENCY RESPONSE WITH VARYING OUTPUT VOLTAGE SWING**

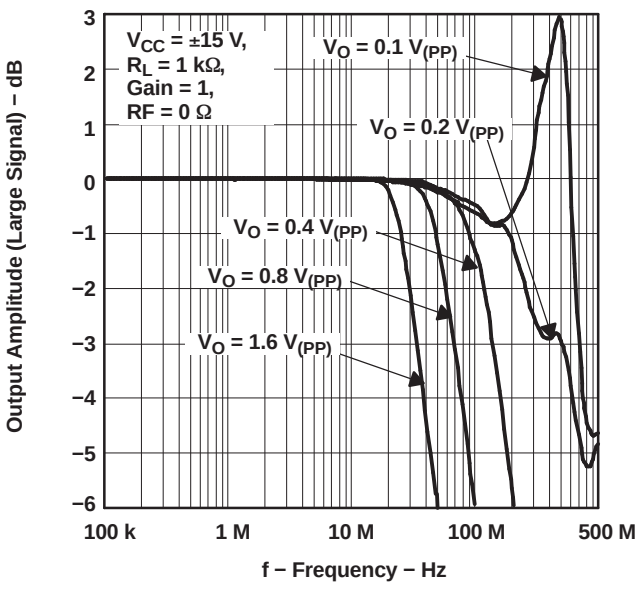



Figure 27.

## TYPICAL CHARACTERISTICS (continued)

SMALL SIGNAL FREQUENCY RESPONSE
WITH VARYING FEEDBACK RESISTANCE

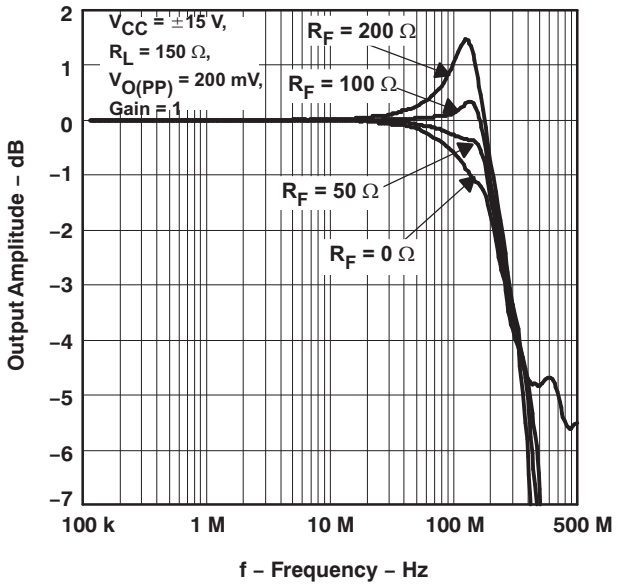



Figure 28.

FREQUENCY RESPONSE WITH
VARYING OUTPUT VOLTAGE SWING

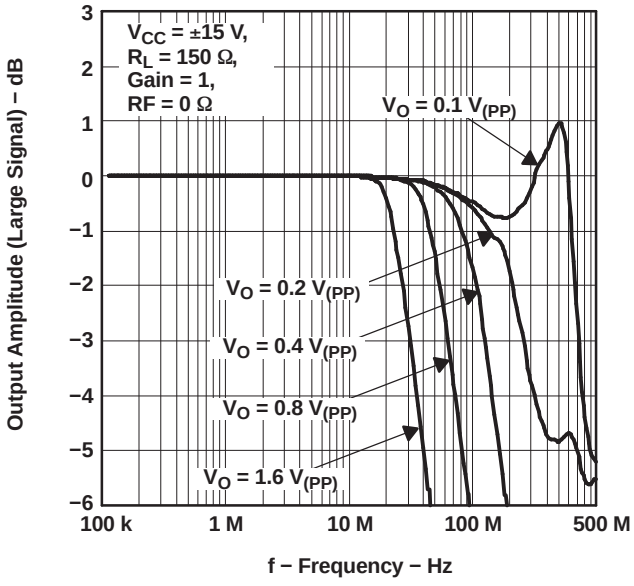



Figure 29.

SMALL SIGNAL FREQUENCY RESPONSE
WITH VARYING FEEDBACK RESISTANCE

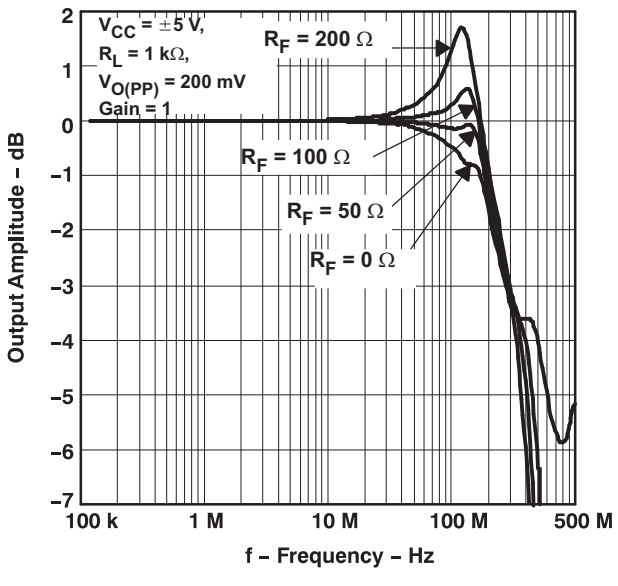



Figure 30.

FREQUENCY RESPONSE WITH
VARYING OUTPUT VOLTAGE SWING

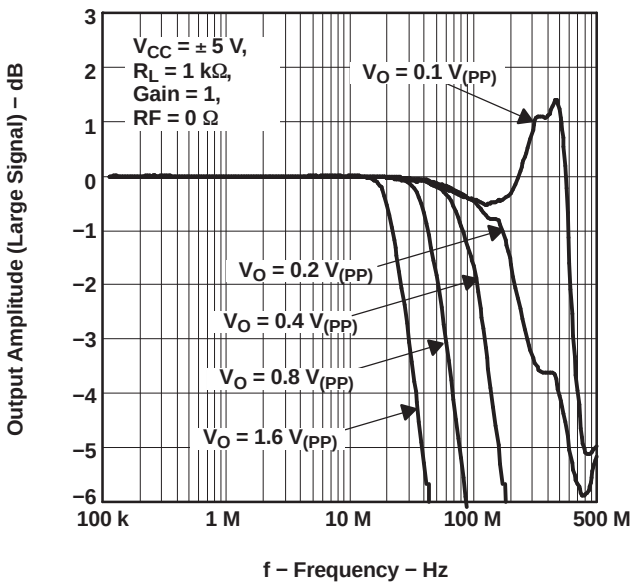



Figure 31.

## TYPICAL CHARACTERISTICS (continued)

SMALL SIGNAL FREQUENCY RESPONSE
WITH VARYING FEEDBACK RESISTANCE

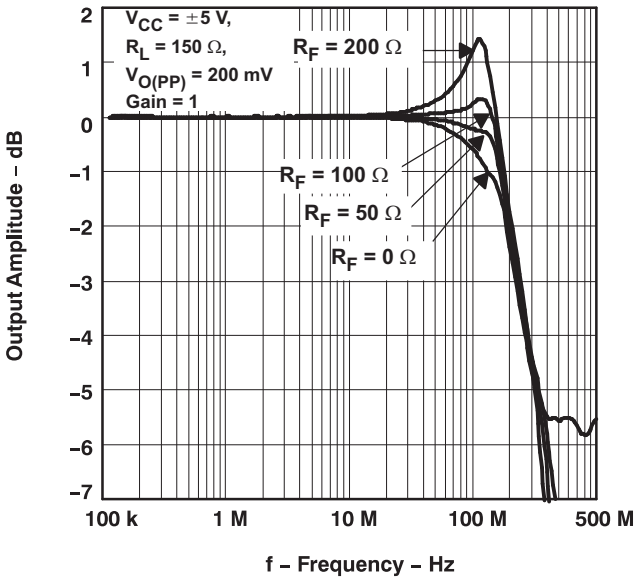



Figure 32.

FREQUENCY RESPONSE WITH
VARYING OUTPUT VOLTAGE SWING

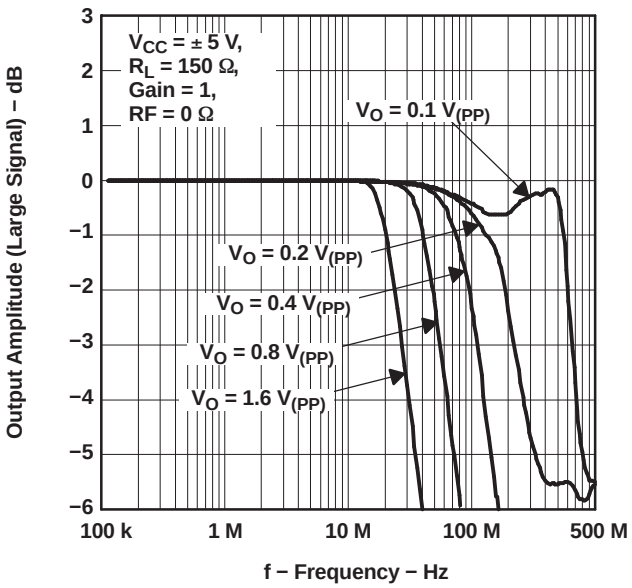



Figure 33.

SMALL SIGNAL FREQUENCY RESPONSE
WITH VARYING FEEDBACK RESISTANCE

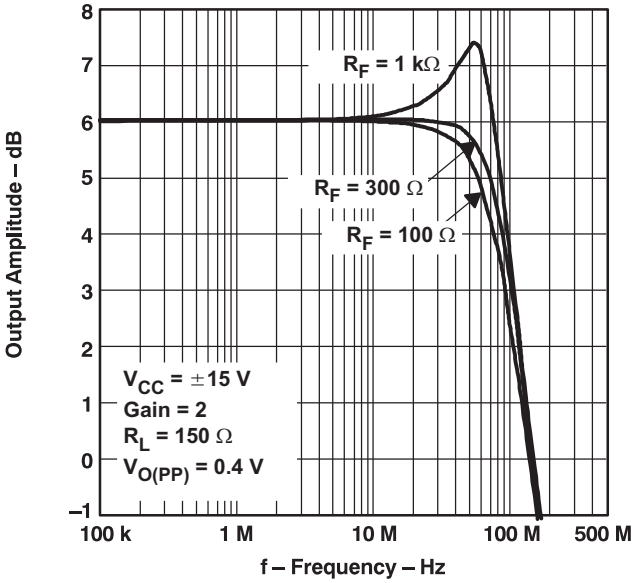



Figure 34.

SMALL SIGNAL FREQUENCY RESPONSE
WITH VARYING FEEDBACK RESISTANCE

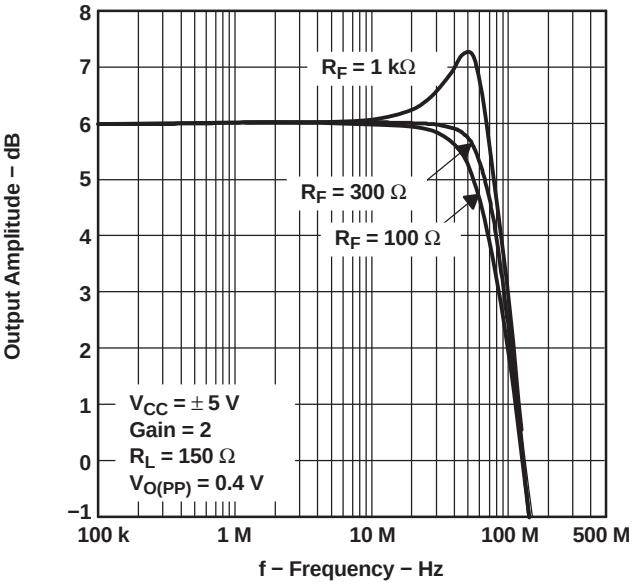



Figure 35.

## TYPICAL CHARACTERISTICS (continued)

SMALL SIGNAL FREQUENCY RESPONSE
WITH VARYING FEEDBACK RESISTANCE

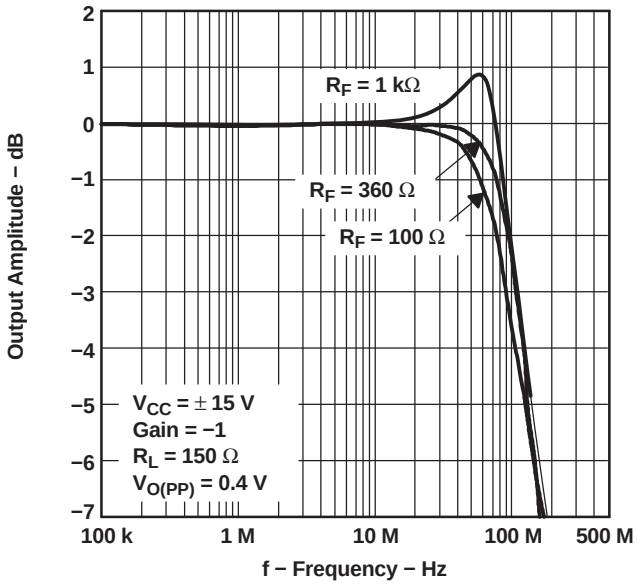



Figure 36.

SMALL SIGNAL FREQUENCY RESPONSE
WITH VARYING FEEDBACK RESISTANCE

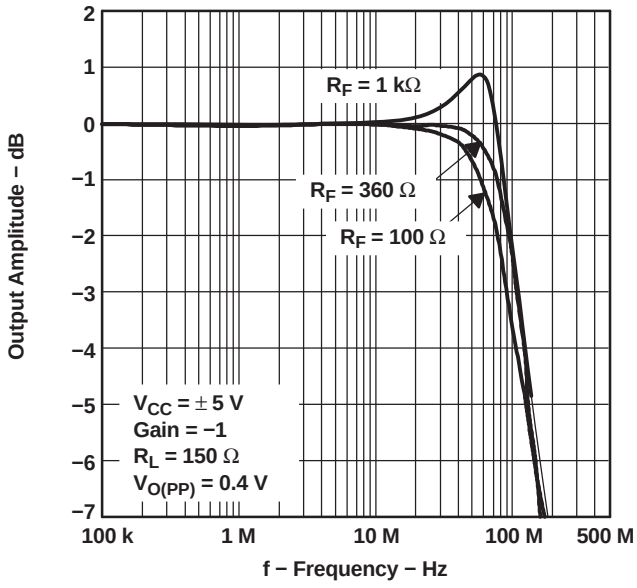



Figure 37.

SMALL SIGNAL
FREQUENCY RESPONSE

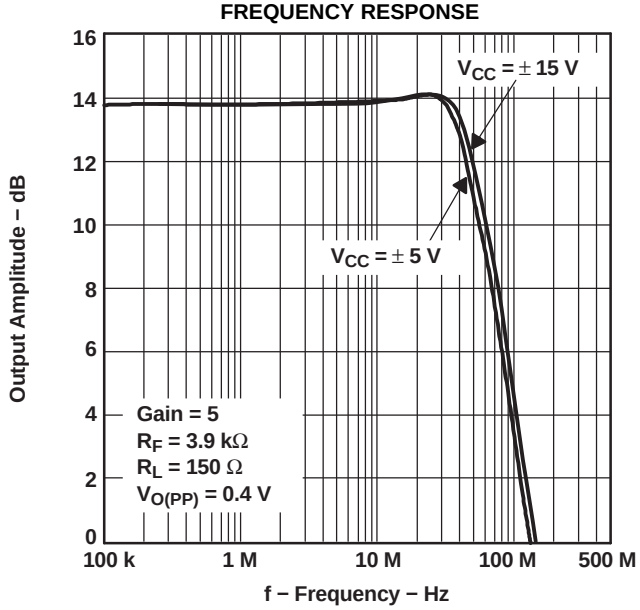



Figure 38.

## TYPICAL CHARACTERISTICS (continued)

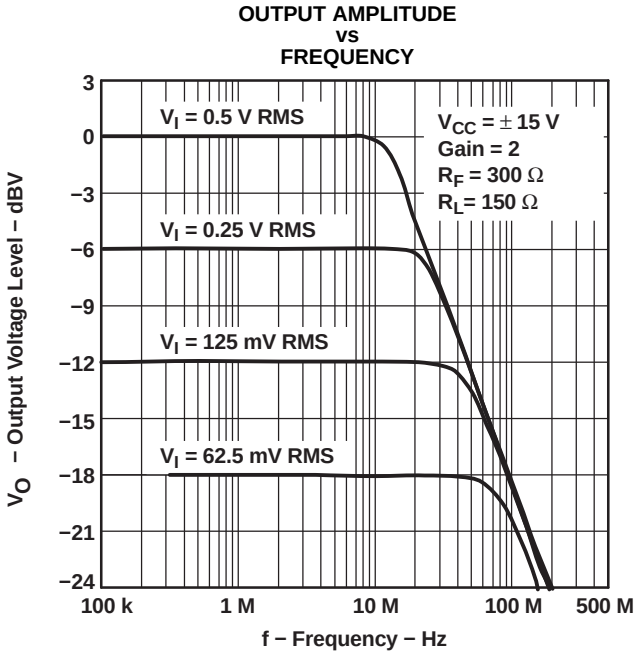



Figure 39.

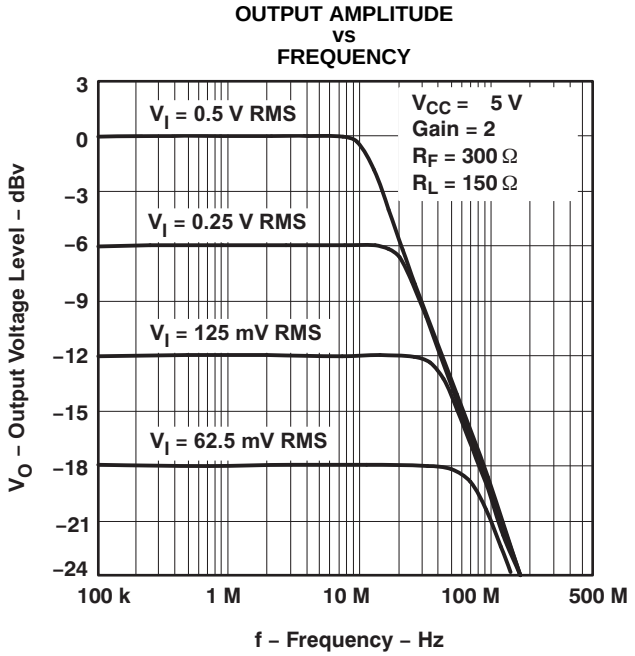



Figure 40.

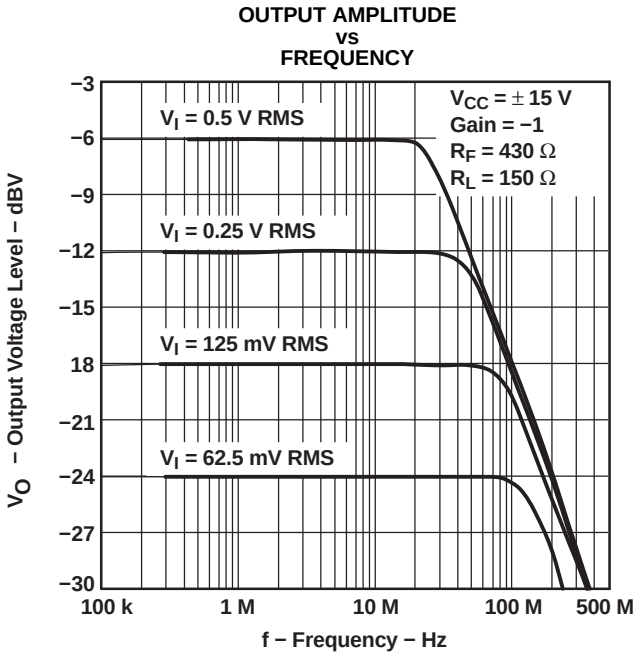



Figure 41.

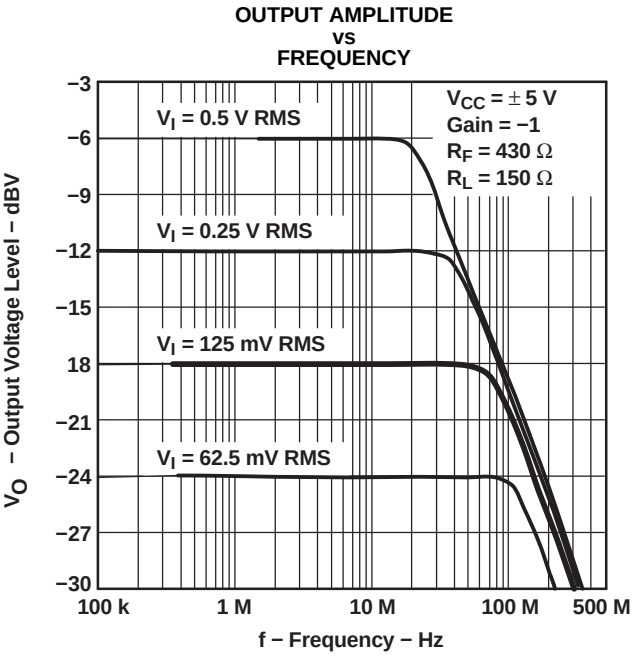



Figure 42.

## TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL PHASE
vs
NUMBER OF 150-Ω LOADS

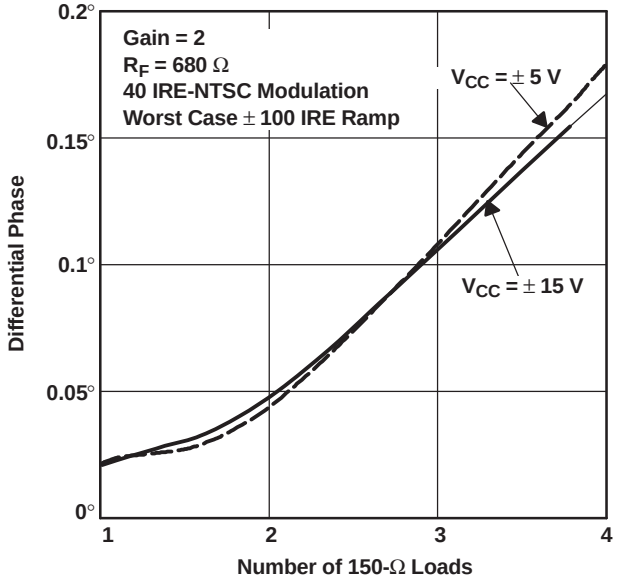



Figure 43.

DIFFERENTIAL PHASE
vs
NUMBER OF 150-Ω LOADS

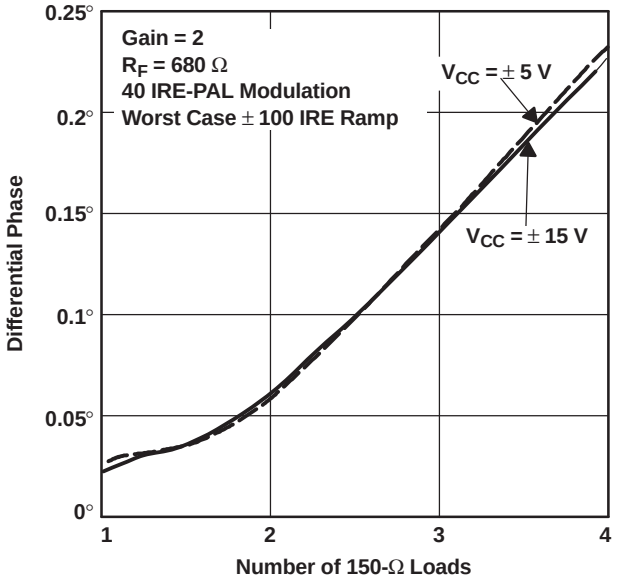



Figure 44.

DIFFERENTIAL GAIN
vs
NUMBER OF 150-Ω LOADS

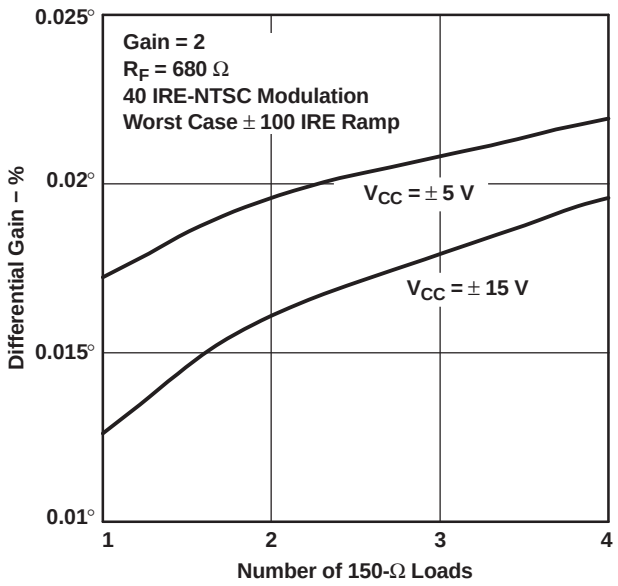



Figure 45.

DIFFERENTIAL GAIN
vs
NUMBER OF 150-Ω LOADS

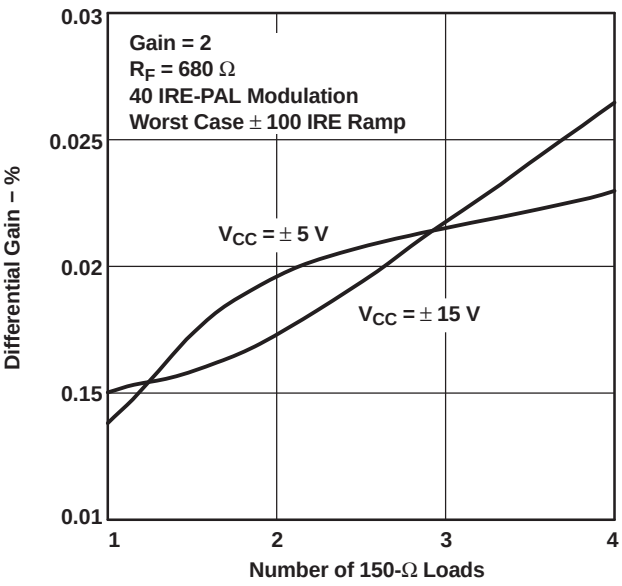



Figure 46.

## TYPICAL CHARACTERISTICS (continued)

1-V STEP RESPONSE

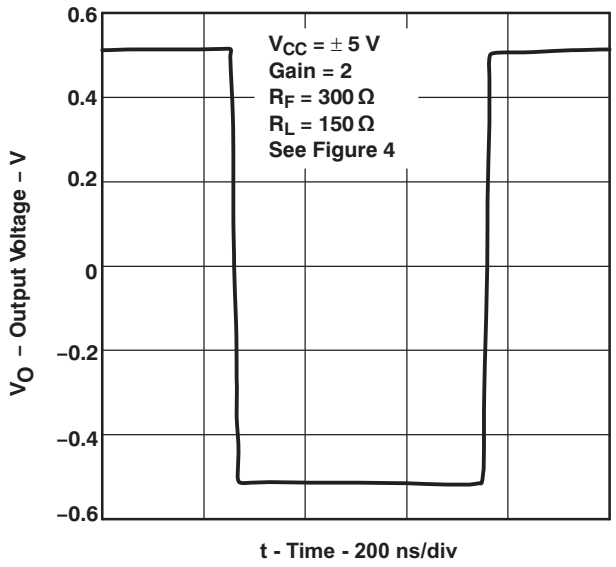



Figure 47.

1-V STEP RESPONSE

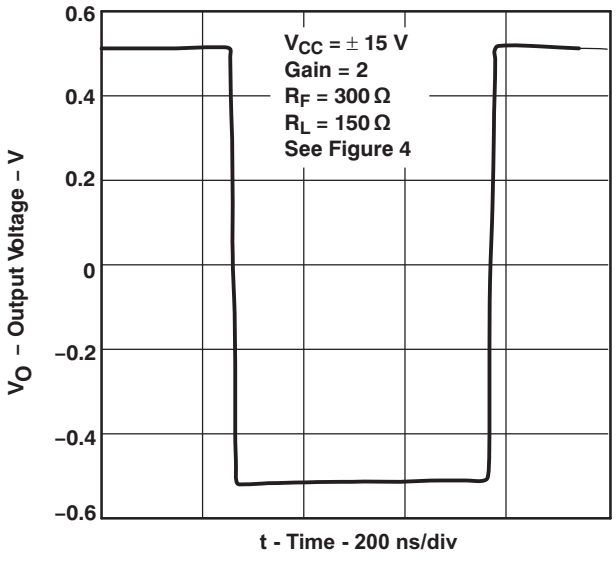



Figure 48.

4-V STEP RESPONSE

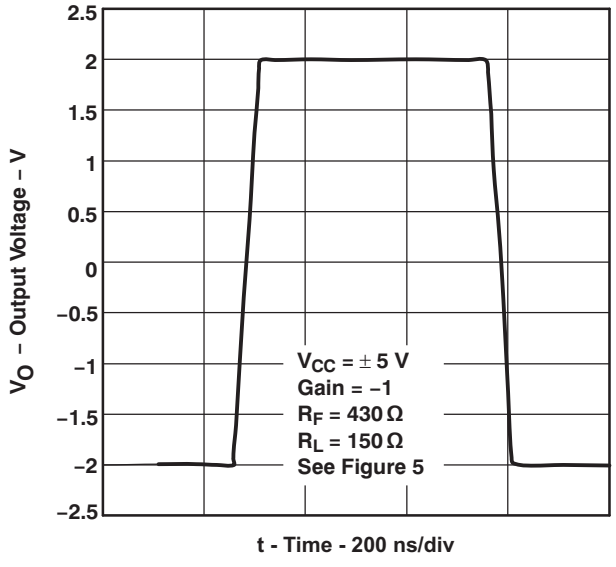



Figure 49.

20-V STEP RESPONSE

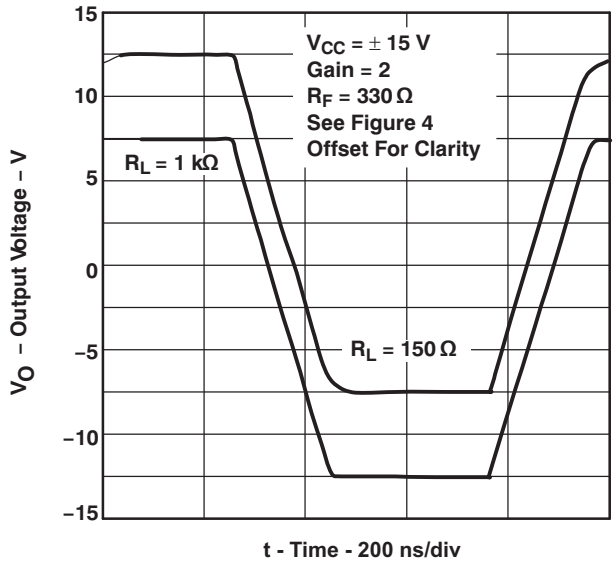



Figure 50.

## APPLICATION INFORMATION

### THEORY OF OPERATION

The THS403x is a high-speed operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing $f_T$s of several GHz. This results in an exceptionally high-performance amplifier that has wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 51.

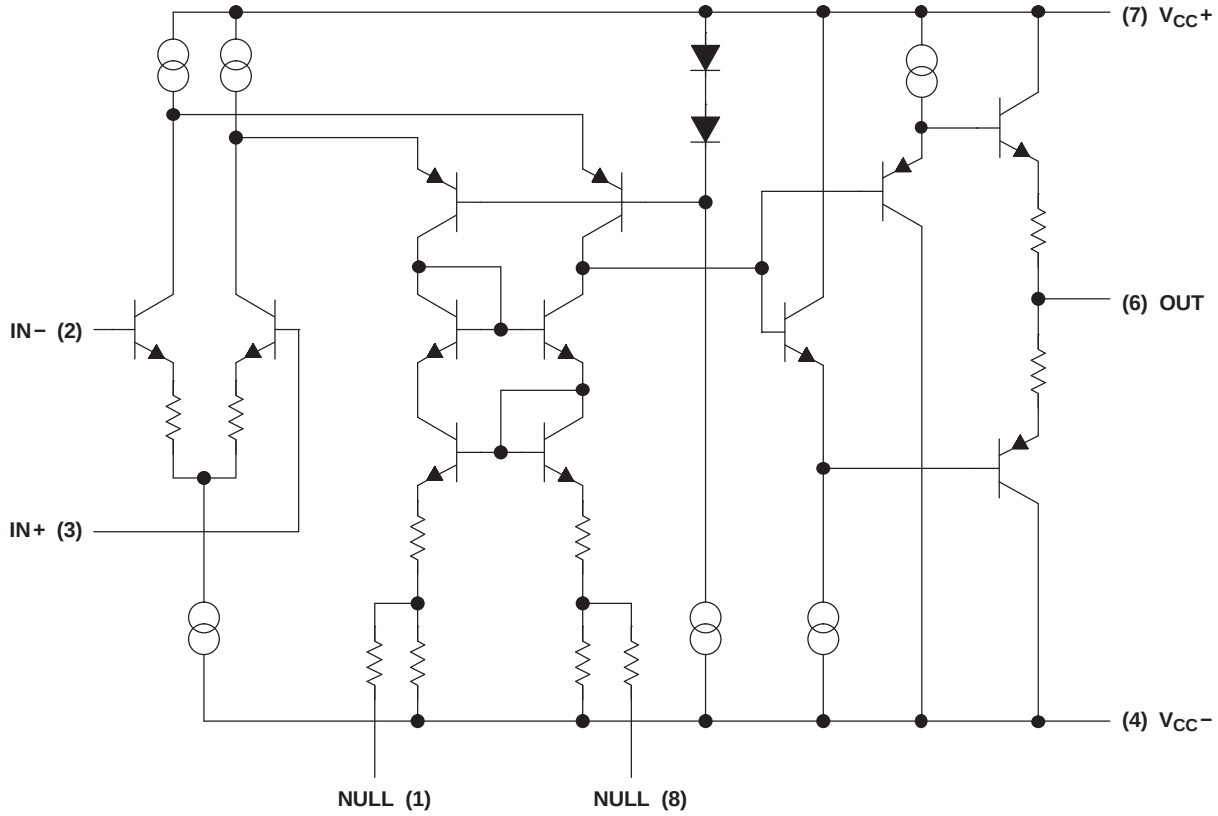



**Figure 51. THS4031 Simplified Schematic**

## NOISE CALCULATIONS AND NOISE FIGURE

Noise can cause errors on very small signals. This is especially true when amplifying small signals. The noise model for the THS403x, shown in Figure 52, includes all of the noise sources as follows:

- $e_n$ = Amplifier internal voltage noise (nV/√Hz)
- IN+ = Noninverting current noise (pA/√Hz)
- IN– = Inverting current noise (pA/√Hz)
- $e_{Rx}$ = Thermal voltage noise associated with each resistor ($e_{Rx}$ = 4 kT$R_x$)

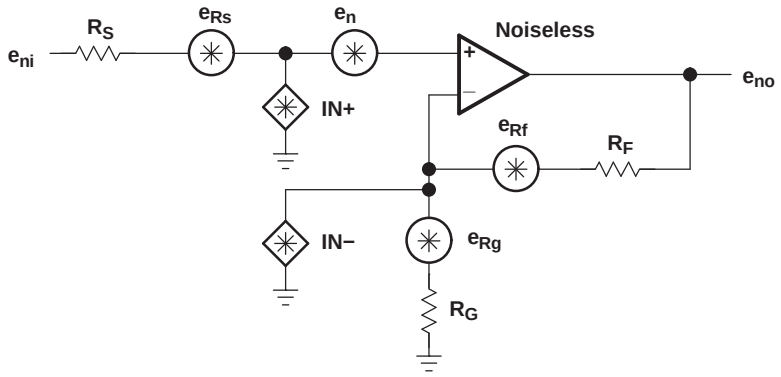



**Figure 52. Noise Model**

The total equivalent input noise density ($e_{ni}$) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN + \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\,kTR_S + 4\,kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = $1.380658 \times 10^{-23}$
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of $R_F$ and $R_G$ (1)

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density ($e_{ni}$) by the overall amplifier gain ($A_V$).

$$e_{no} = e_{ni}\,A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)} \quad (2)$$

As the previous equations show, to keep noise at a minimum, small-value resistors should be used. As the closed-loop gain is increased (by reducing $R_G$), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor ($R_S$) and the internal amplifier noise voltage ($e_n$). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This advantage can greatly simplify the formula and make noise calculations much easier to calculate.

For more information on noise analysis, refer to the application note, *Noise Analysis for High-Speed Op Amps* (SBOA066).

## OPTIMIZING FREQUENCY RESPONSE

Internal frequency compensation of the THS403x was selected to provide very wide bandwidth performance and still maintain a very low noise floor. In order to meet these performance requirements, the THS403x must have a minimum gain of 2 (–1). Because everything is referred to the noninverting terminal of an operational amplifier, the noise gain in a G = –1 configuration is the same as a G = 2 configuration.

One of the keys to maintaining a smooth frequency response, and hence, a stable pulse response, is to pay particular attention to the inverting terminal. Any stray capacitance at this node causes peaking in the frequency response (see Figure 53 and Figure 54). Two things can be done to help minimize this effect. The first is to simply remove any ground planes under the inverting terminal of the amplifier, including the trace that connects to this terminal. Additionally, the length of this trace should be minimized. The capacitance at this node causes a lag in the voltage being fed back due to the charging and discharging of the stray capacitance. If this lag becomes too long, the amplifier will not be able to correctly keep the noninverting terminal voltage at the same potential as the inverting terminal's voltage. Peaking and possible oscillations will then occur if this happens.

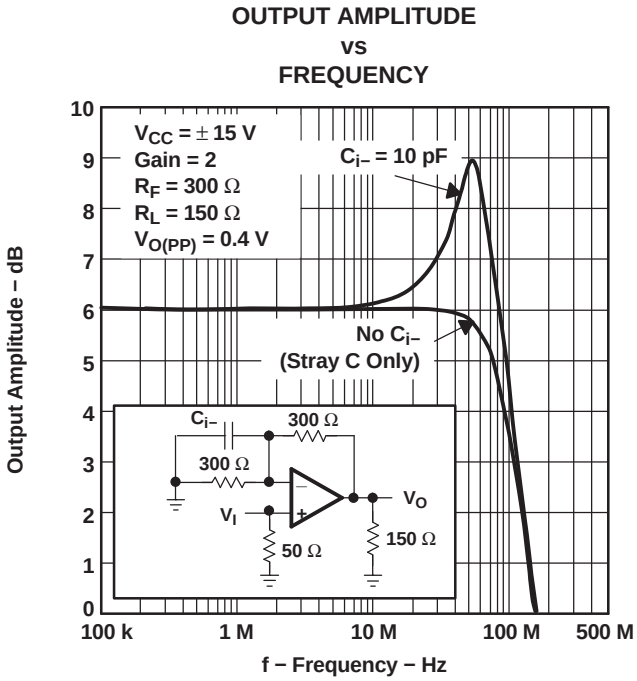



**Figure 53.**

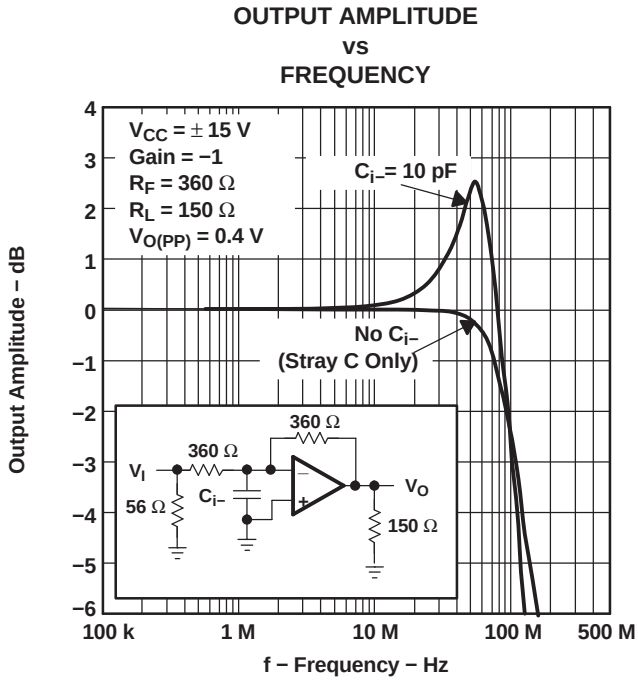



**Figure 54.**

The second precaution to help maintain a smooth frequency response is to keep the feedback resistor ($R_f$) and the gain resistor ($R_g$) values fairly low. These two resistors are effectively in parallel when looking at the ac small-signal response. But, as can be seen in Figure 26 through Figure 37, a value too low starts to reduce the bandwidth of the amplifier. Table 1 shows some recommended feedback resistors to be used with the THS403x.

**Table 1. Recommended Feedback Resistors**

| GAIN | $R_f$ for $V_{CC}$ = ±15 V and ±5 V |
|---|---|
| 1 | 50 Ω |
| 2 | 300 Ω |
| –1 | 360 Ω |
| 5 | 3.3 kΩ (low stray-c PCB only) |

## DRIVING A CAPACITIVE LOAD

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS403x has been internally compensated to maximize its bandwidth and slew-rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the phase margin of the device leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 55. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

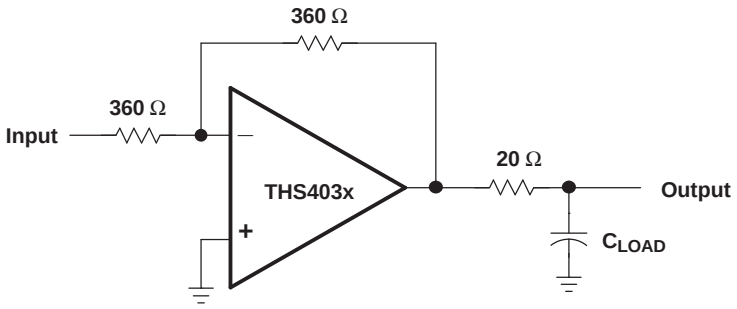



**Figure 55. Driving a Capacitive Load**

## OFFSET NULLING

The THS403x has very low input offset voltage for a high speed amplifier. However, if additional correction is required, the designer can make use of an offset nulling function provided on the THS4031. By placing a potentiometer between terminals 1 and 8 of the device and tying the wiper to the negative supply, the input offset can be adjusted. This is shown in Figure 56.

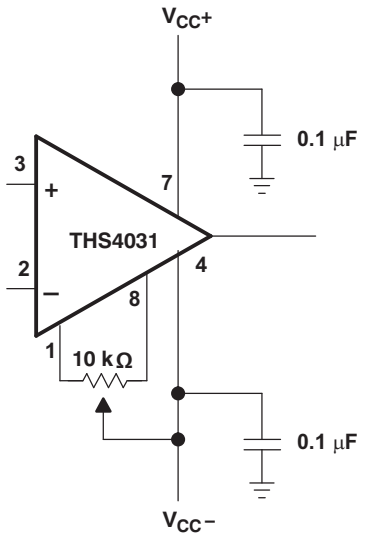
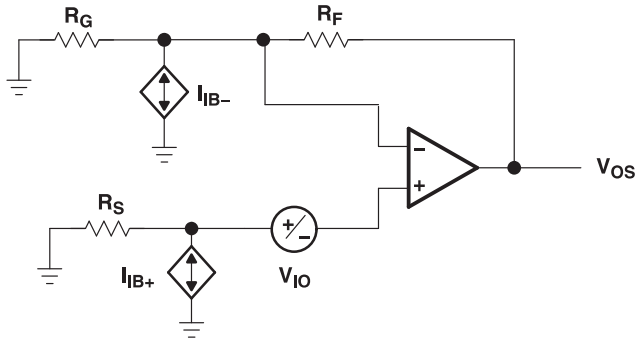



**Figure 56. Offset Nulling Schematic**

## OFFSET VOLTAGE

The output offset voltage ($V_{OO}$) is the sum of the input offset voltage ($V_{IO}$) and both input bias currents ($I_{IB}$) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:




$$V_{OS} = \left(\pm V_{IO} \pm I_{IB+} R_S\right)\left(1 + \frac{R_F}{R_G}\right) \pm I_{IB-} R_F$$

**Figure 57. Output Offset Voltage Model**

## GENERAL CONFIGURATIONS

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifer (see Figure 58).

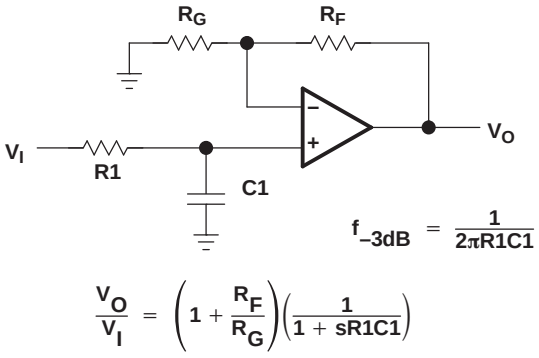



**Figure 58. Single-Pole Low-Pass Filter**

If even more attenuation is needed, a multiple-pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Otherwise, phase shift of the amplifier can occur.

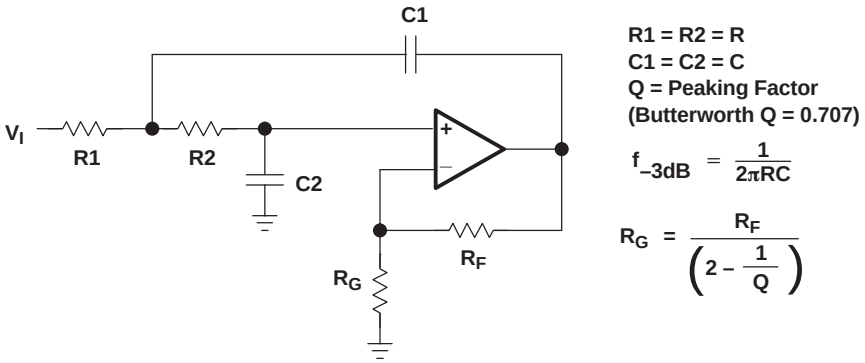



**Figure 59. Two-Pole Low-Pass Sallen-Key Filter**

## CIRCUIT-LAYOUT CONSIDERATIONS

In order to achieve the levels of high-frequency performance of the THS403x, it is essential that proper printed-circuit board (PCB) high-frequency design techniques be followed. A general set of guidelines is given below. In addition, a THS403x evaluation board is available to use as a guide for layout or for evaluating the device performance.

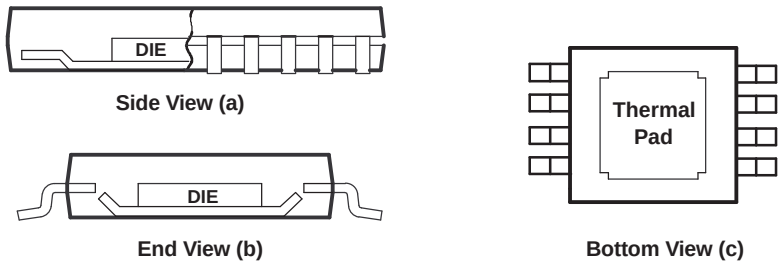
- Ground planes: It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power-supply decoupling: Use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inch between the device power terminals and the ceramic capacitors.
- Sockets: Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements: Optimum high-frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components: Using surface-mount passive components is recommended for high-frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

## GENERAL PowerPAD™ DESIGN CONSIDERATIONS

The THS403x is available in a thermally-enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 60(a) and Figure 60(b)]. This arrangement results in the leadframe being exposed as a thermal pad on the underside of the package [see Figure 60(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the heretofore awkward mechanical methods of heatsinking.




A. The thermal pad is electrically isolated from all terminals in the package.

**Figure 60. Views of Thermally-Enhanced DGN Package**

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach.

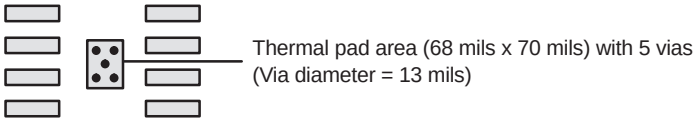



**Figure 61. PowerPAD™ PCB Etch and Via Pattern**

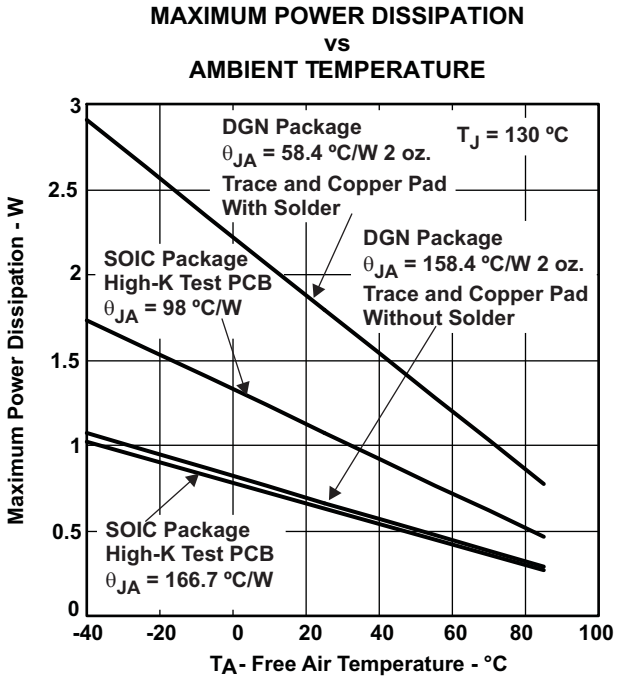
1. Prepare the PCB with a top-side etch pattern as shown in Figure 61. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils (0,3302 mm) in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS403xDGN IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, *do not* use the typical web or spoke via connection methodology. Web connections have a high thermal-resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS403xDGN package should connect to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area, which prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and to all the IC terminals.
8. With these preparatory steps in place, the THS403xDGN IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

The actual thermal performance achieved with the THS403xDGN in its PowerPAD™ package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches × 3 inches (7,62 cm × 7,62 cm), then the expected thermal coefficient, $\theta_{JA}$, is about 58.4°C/W. For comparison, the non-PowerPAD™ version of the THS403x IC (SOIC) is shown. For a given $\theta_{JA}$, the maximum power dissipation is shown in Figure 62 and is calculated by the following formula:

$$P_D = \left( \frac{T_{MAX} - T_A}{\theta_{JA}} \right) \quad (3)$$

Where:

$P_D$ = Maximum power dissipation of THS403x IC (watts)
$T_{MAX}$ = Absolute maximum operating junction temperature (125°C)
$T_A$ = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
$\theta_{JC}$ = Thermal coefficient from junction to case
$\theta_{CA}$ = Thermal coefficient from case to ambient air (°C/W)




Results are with no air flow and PCB size = 3”ɔ3” (7,62 cm x 7,62 cm)

**Figure 62. Maximum Power Dissipation vs Free-Air Temperature**

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments technical brief, *PowerPAD™ Thermally-Enhanced Package* (SLMA002). This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

The next thing to be considered is package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multiamplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. Figure 63 to Figure 66 shows this effect, along with the quiescent heat, with an ambient air temperature of 50°C. When using $V_{CC}$ = ±5 V, heat is generally not a problem, even with SOIC packages. But, when using $V_{CC}$ = ±15 V, the SOIC package is severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD™ devices are extremely useful for heat dissipation. But, the device should

always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD™. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, $\theta_{JA}$ decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual amplifier package (THS4032), the sum of the RMS output currents and voltages should be used to choose the proper package.

**MAXIMUM RMS OUTPUT CURRENT vs RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS**

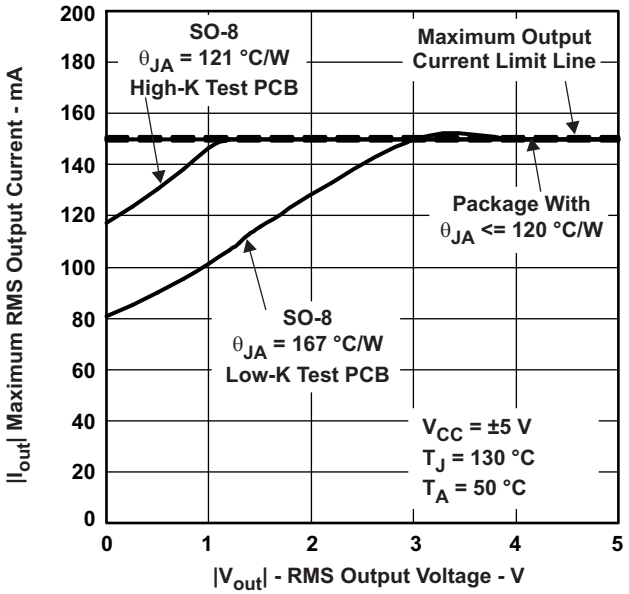



Figure 63.

**MAXIMUM RMS OUTPUT CURRENT vs RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS**

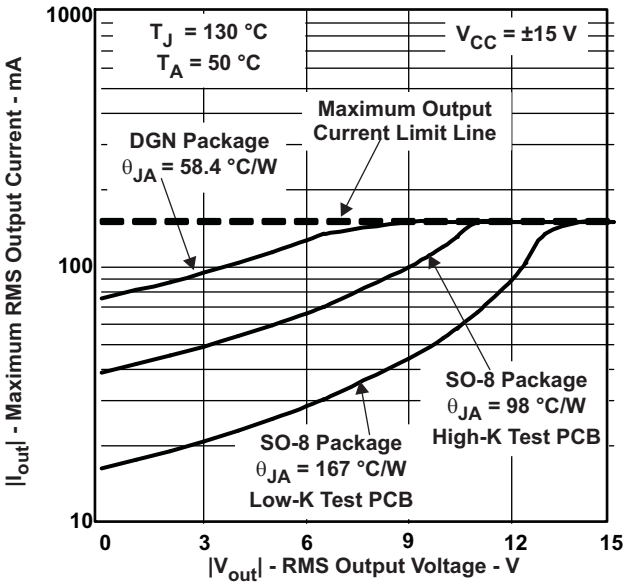



Figure 64.

**MAXIMUM RMS OUTPUT CURRENT vs RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS**

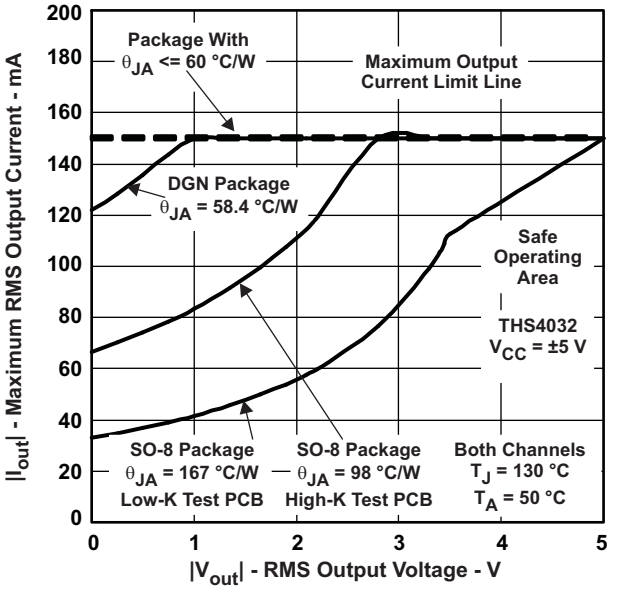



Figure 65.

**MAXIMUM RMS OUTPUT CURRENT vs RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS**

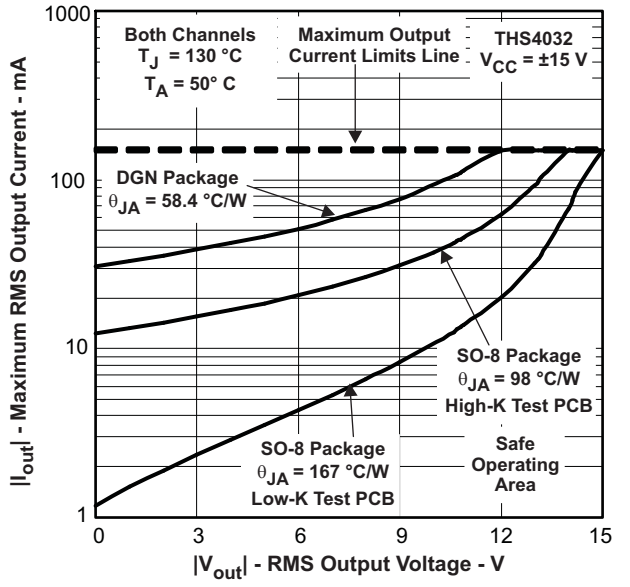



Figure 66.

## EVALUATION BOARD

An evaluation board is available for the THS4031 (literature number SLOP203) and THS4032 (literature number SLOP135). This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the evaluation board is shown in Figure 67. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. For more information, refer to the *THS4031 EVM User's Guide* (SLOU038) or the *THS4032 EVM User's Guide* (SLOU039). To order the evaluation board, contact your local TI sales office or distributor.

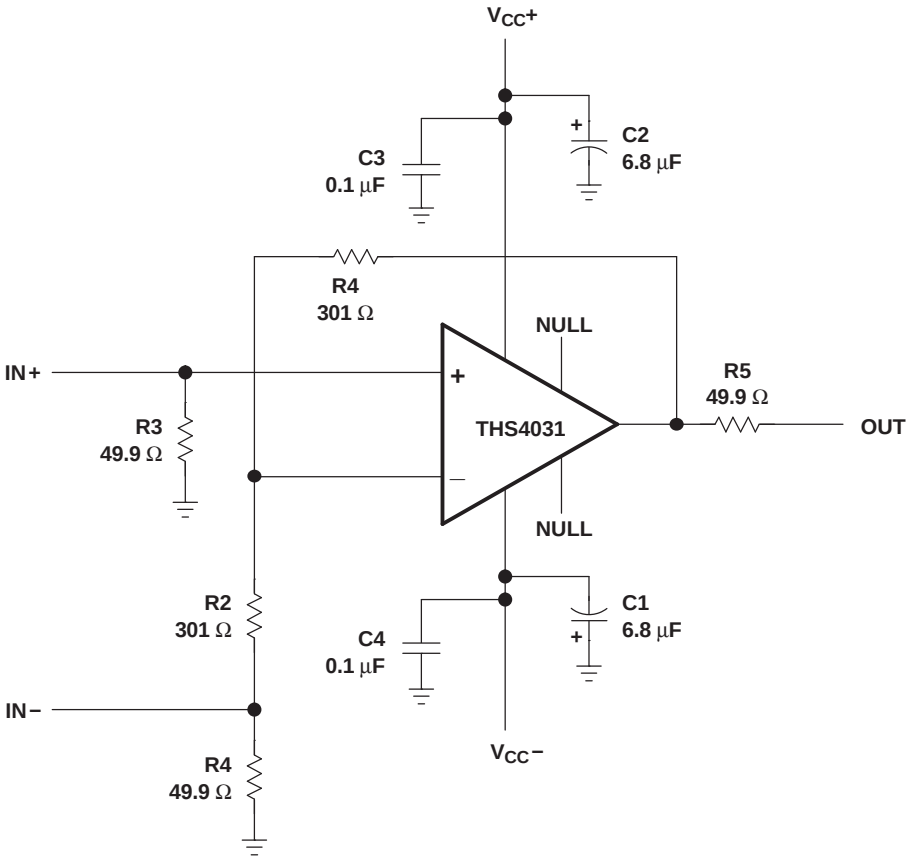



**Figure 67. THS4031 Evaluation Board**

## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision E (June, 2007) to Revision F | Page |
|---|---|
| • Deleted bullet point for *Stable in Gain of 2 (–1) or greater* | 1 |
| • Editorial changes to paragraph format | 28 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| 5962-9959501Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-9959501QPA | ACTIVE | CDIP | JG | 8 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| THS4031CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4031CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4031CDGN | ACTIVE | MSOP-Power PAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4031CDGNG4 | ACTIVE | MSOP-Power PAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4031CDGNR | ACTIVE | MSOP-Power PAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4031CDGNRG4 | ACTIVE | MSOP-Power PAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4031CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4031CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4031ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4031IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4031IDGN | ACTIVE | MSOP-Power PAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4031IDGNG4 | ACTIVE | MSOP-Power PAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4031IDGNR | ACTIVE | MSOP-Power PAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4031IDGNRG4 | ACTIVE | MSOP-Power PAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4031IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4031IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4031MFKB | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| THS4031MJG | ACTIVE | CDIP | JG | 8 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| THS4031MJGB | ACTIVE | CDIP | JG | 8 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| THS4032CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4032CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4032CDGN | ACTIVE | MSOP- | DGN | 8 | 80 | Green (RoHS & | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| | | Power PAD | | | | no Sb/Br) | | |
| THS4032CDGNG4 | ACTIVE | MSOP-Power PAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4032CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4032CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4032ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4032IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4032IDGN | ACTIVE | MSOP-Power PAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4032IDGNG4 | ACTIVE | MSOP-Power PAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4032IDGNR | ACTIVE | MSOP-Power PAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4032IDGNRG4 | ACTIVE | MSOP-Power PAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4032IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS4032IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF THS4031, THS4031M, THS4032 :**

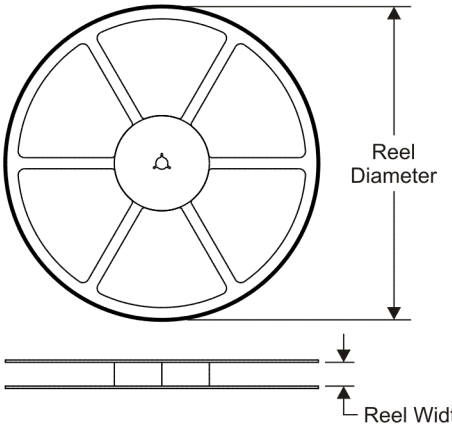
- Enhanced Product: THS4032-EP

NOTE: Qualified Version Definitions:

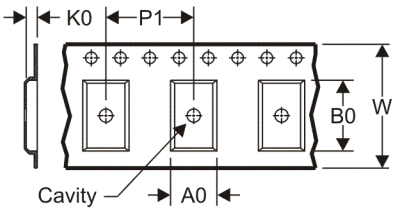
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

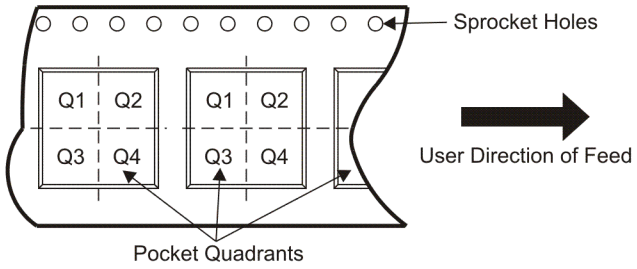



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

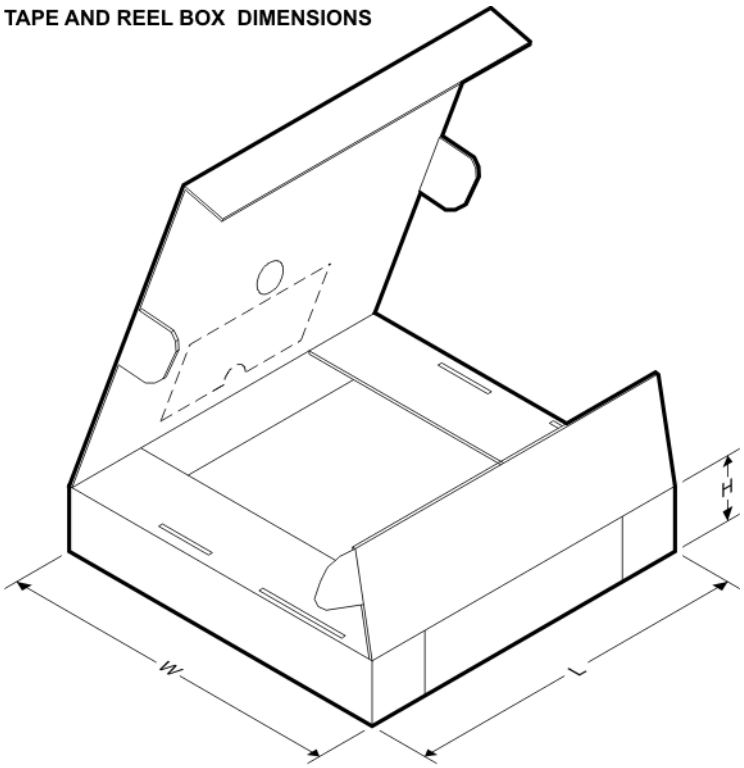
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| THS4031CDGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.2 | 3.3 | 1.6 | 8.0 | 12.0 | Q1 |
| THS4031CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| THS4031IDGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.2 | 3.3 | 1.6 | 8.0 | 12.0 | Q1 |
| THS4031IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| THS4032CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| THS4032IDGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.2 | 3.3 | 1.6 | 8.0 | 12.0 | Q1 |
| THS4032IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**

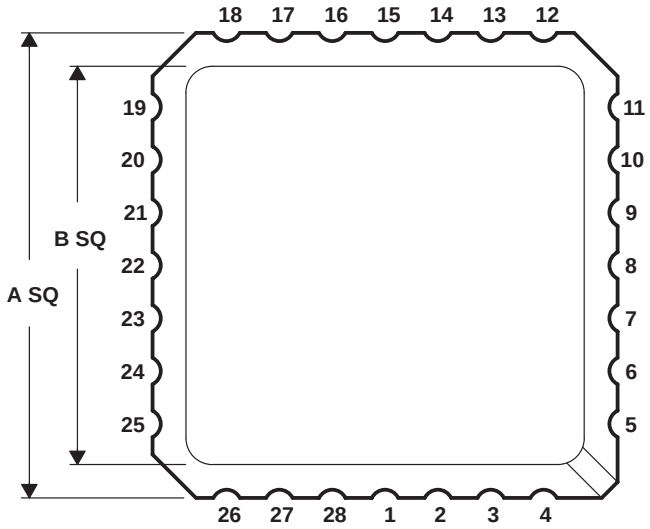



*All dimensions are nominal

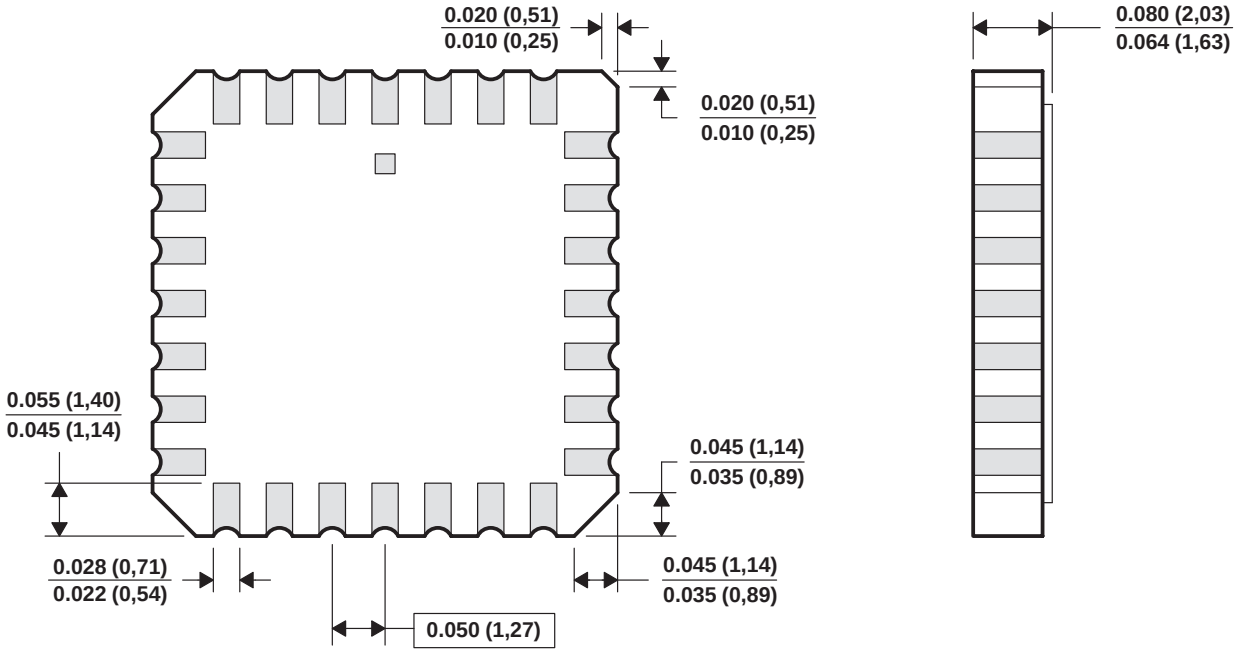
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| THS4031CDGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 338.1 | 340.5 | 21.1 |
| THS4031CDR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |
| THS4031IDGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 338.1 | 340.5 | 21.1 |
| THS4031IDR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |
| THS4032CDR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |
| THS4032IDGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 338.1 | 340.5 | 21.1 |
| THS4032IDR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |

**FK (S-CQCC-N**)** **LEADLESS CERAMIC CHIP CARRIER**

**28 TERMINAL SHOWN**



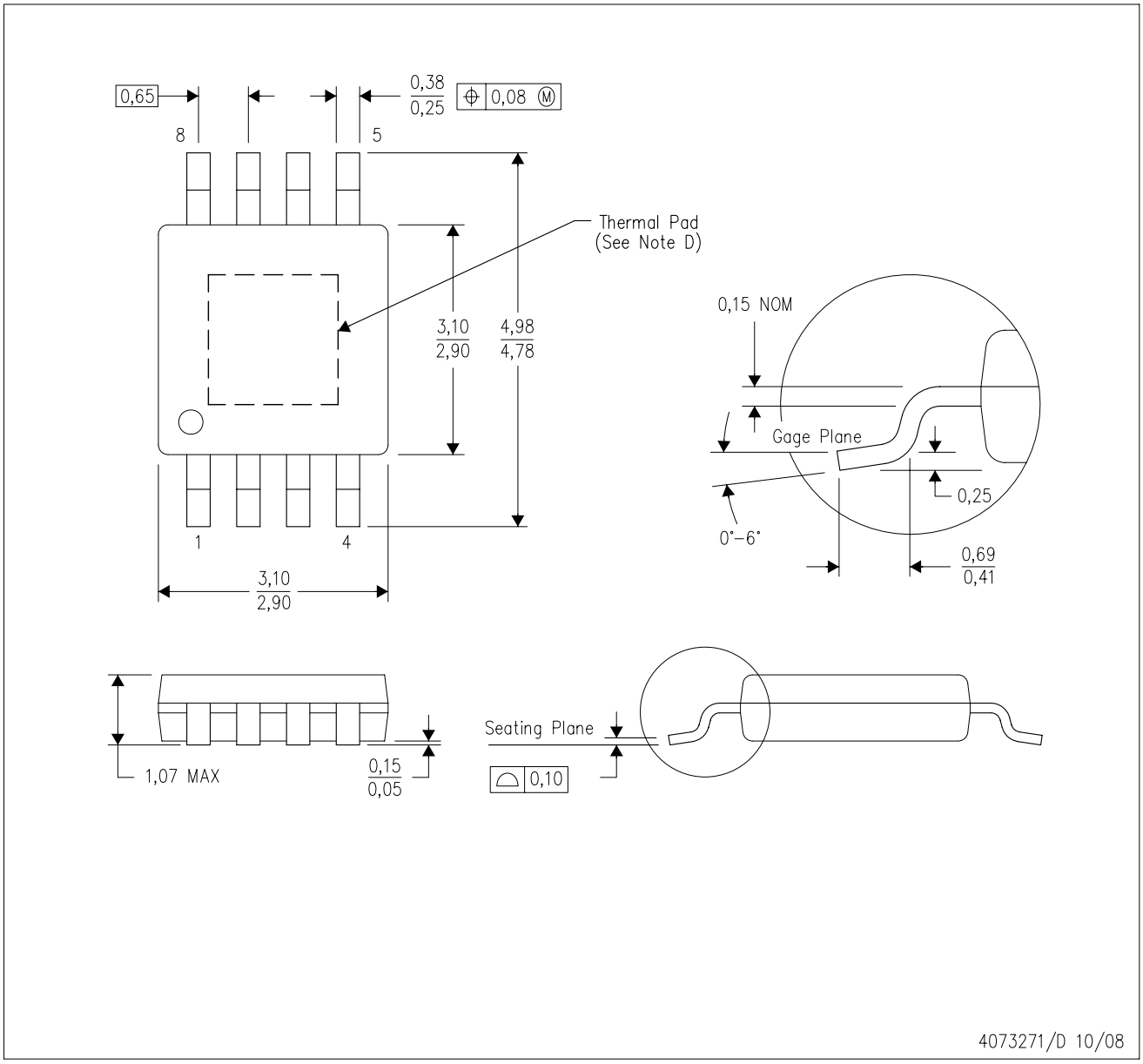

| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.739 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |




**4040140/D 10/96**

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–187

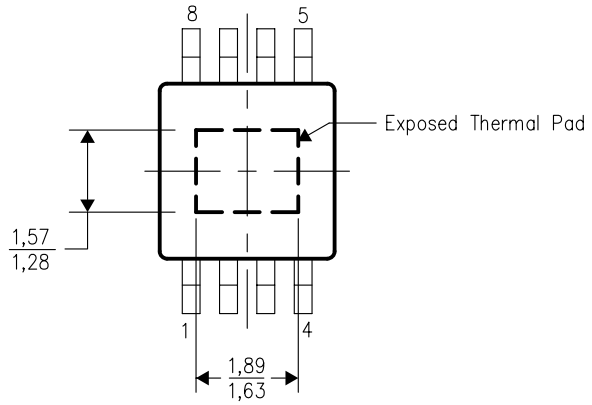
**PowerPAD is a trademark of Texas Instruments.**

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

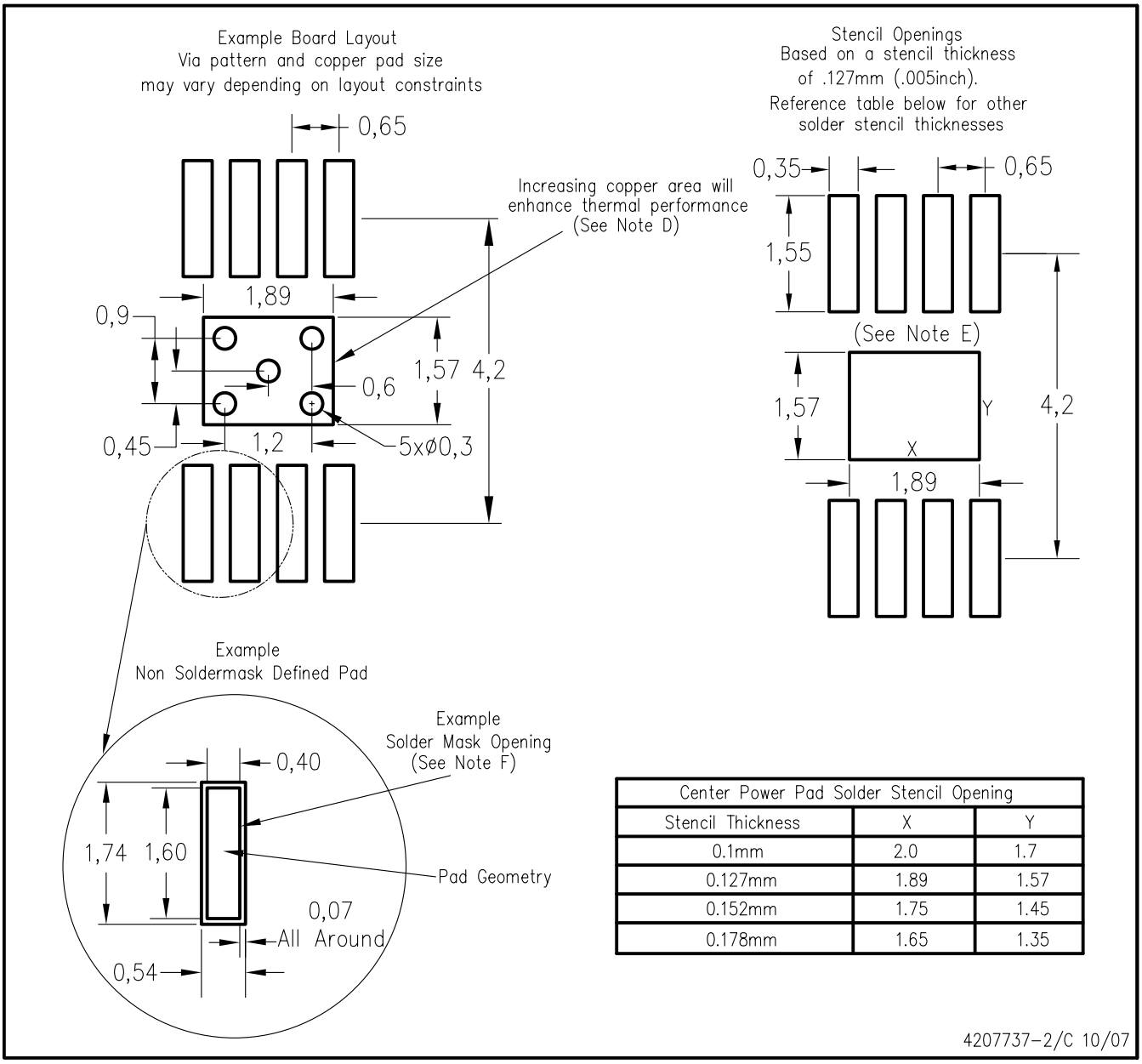



Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

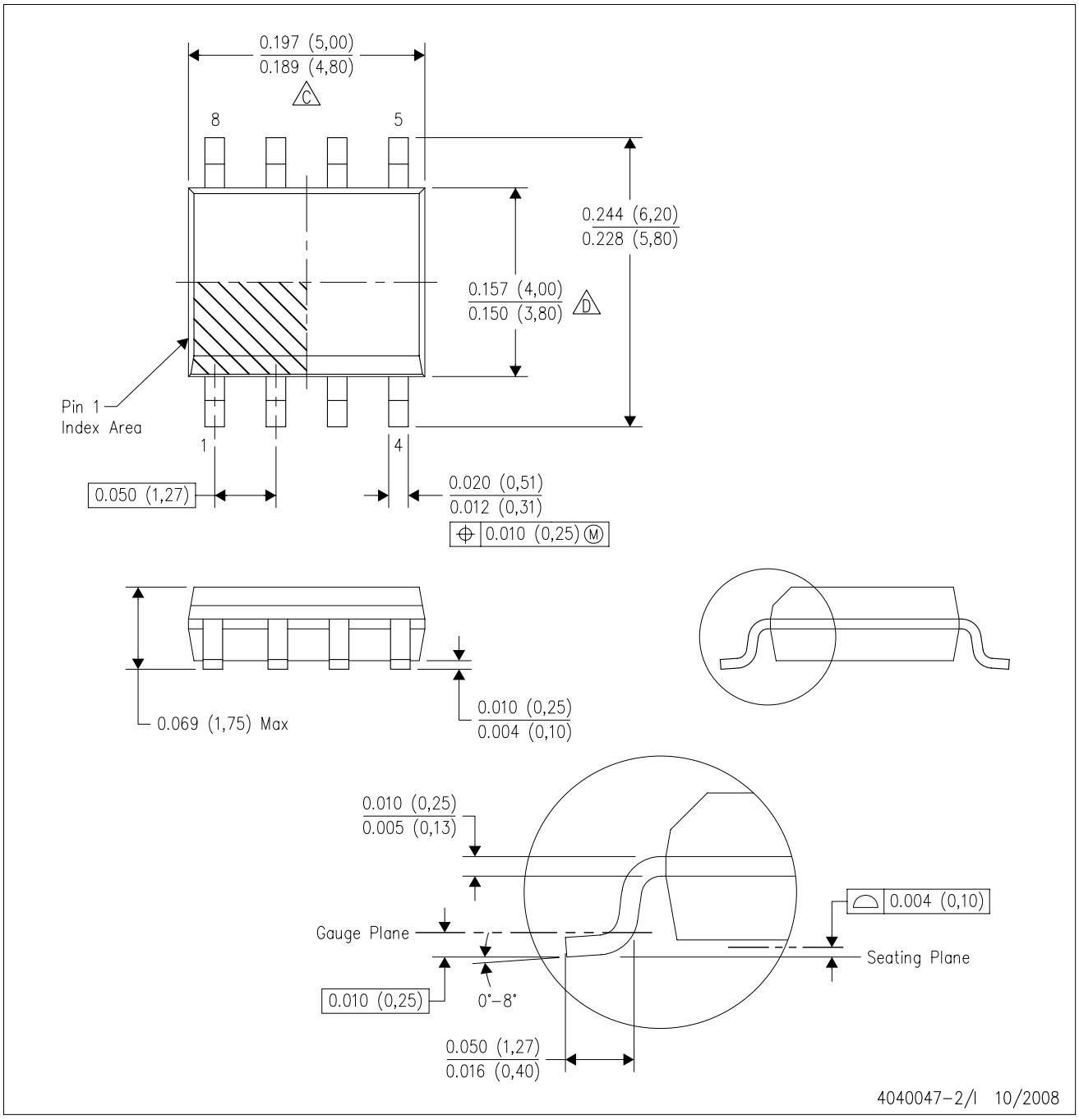
# DGN (R–PDSO–G8) PowerPAD™




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.0 | 1.7 |
| 0.127mm | 1.89 | 1.57 |
| 0.152mm | 1.75 | 1.45 |
| 0.178mm | 1.65 | 1.35 |

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

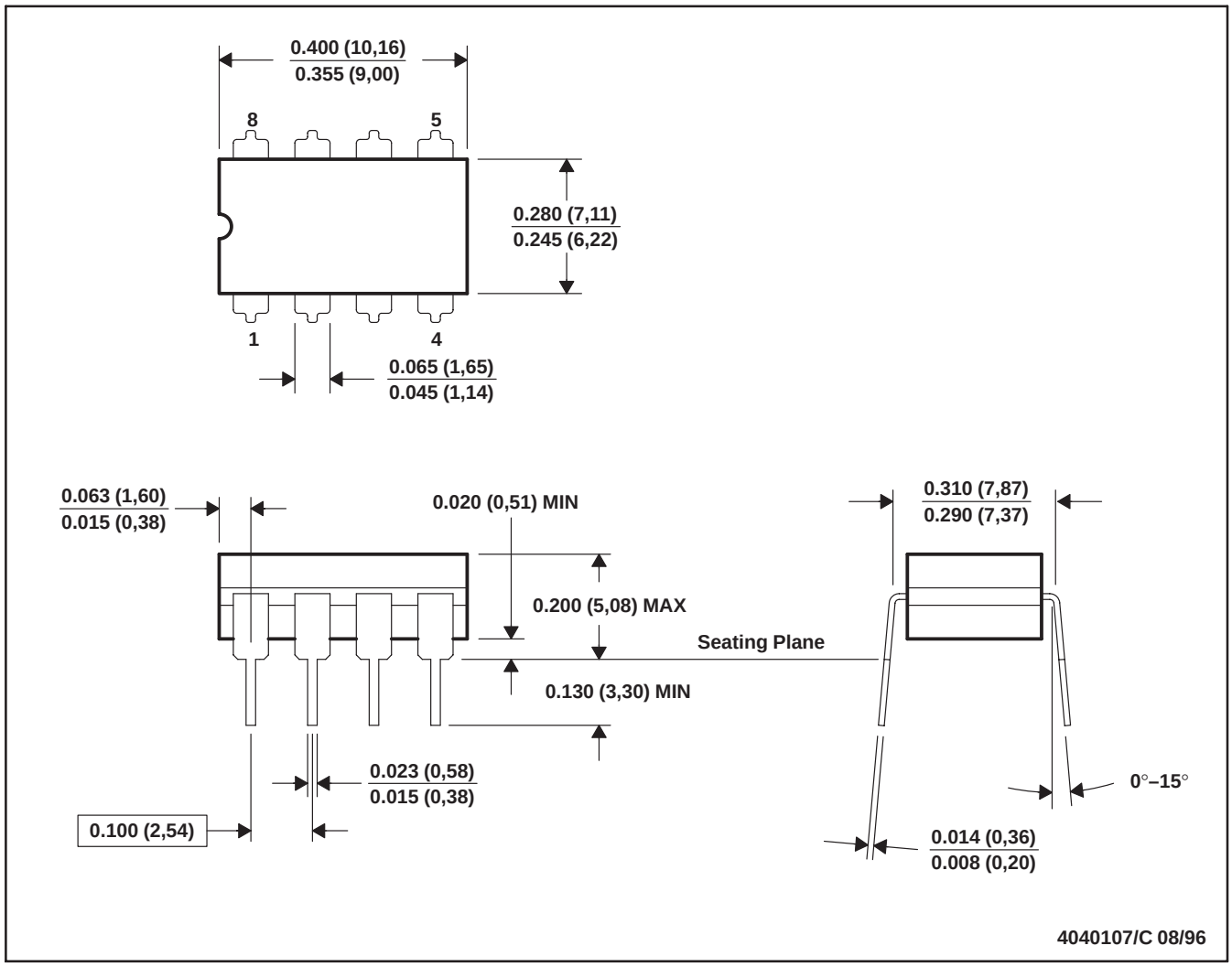
D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

**JG (R-GDIP-T8)** **CERAMIC DUAL-IN-LINE**




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| **Products** | | **Applications** | |
|---|---|---|---|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Clocks and Timers | www.ti.com/clocks | Digital Control | www.ti.com/digitalcontrol |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| RFID | www.ti-rfid.com | Telephony | www.ti.com/telephony |
| RF/IF and ZigBee® Solutions | www.ti.com/lprf | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265