Ordering number : EN 3884B

CMOS LSI

SANYO

No. 3884B

LC7883K, LC7883KM

16-bit Digital Filter and Digital-to-analog Converters for Digital Audio

Overview

The LC7883K and LC7883KM are 16-bit digital filter and digital-to-analog (D/A) converter ICs for digital-audio applications. They comprise a D/A converter and a digital filter with eight times over-sampling for deemphasis and attenuation. The D/A converter uses dynamic level-shifting conversion and does not require an external sample-and-hold circuit. It features zero phase error between channel outputs.

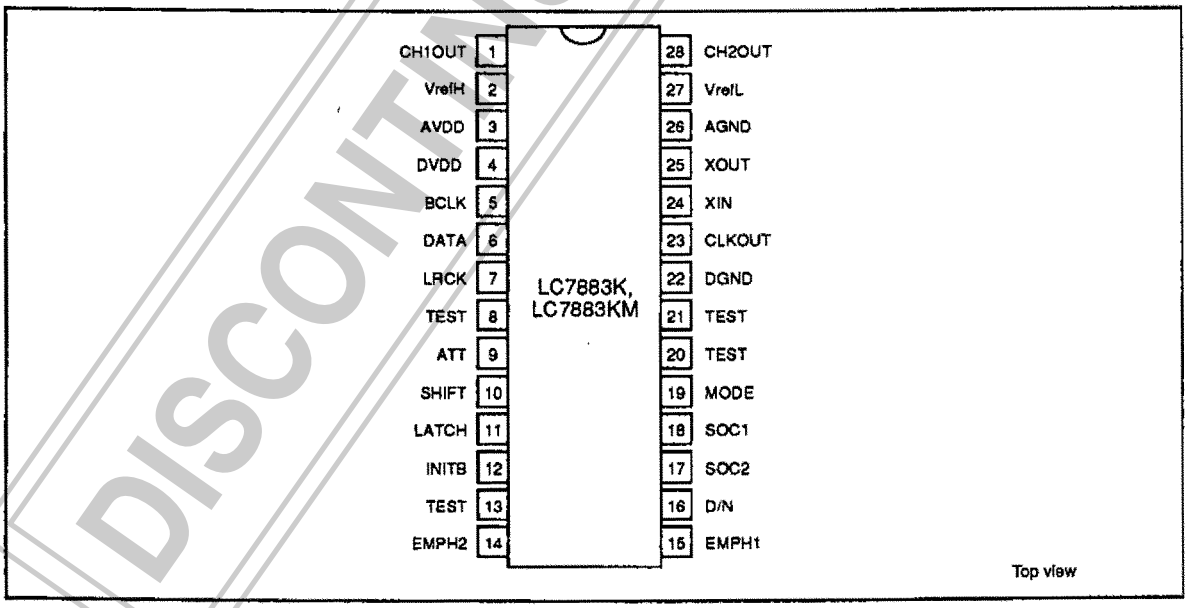
The LC7883K and LC7883KM support different serial data rates—384F_S and 392F_S for CD, 448F_S for CD-ROM, and 512F_S for BS and DAT.

The LC7883K and LC7883KM operate from a 5 V supply and are available in 28-pin MFPs and 28-pin DIPs.

Features

- Dynamic level-shifting digital-to-analog converter
- Supports double-rate sampling
- 2s complement serial input data
- Does not require an external sample-and-hold circuit
- 5 V supply
- 28-pin DIP and 28-pin MFP

Pin Assignment



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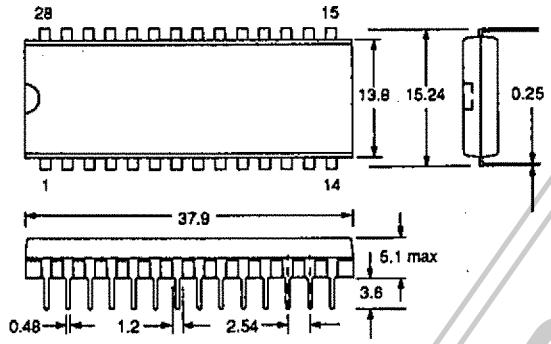
Package Dimensions

Unit: mm

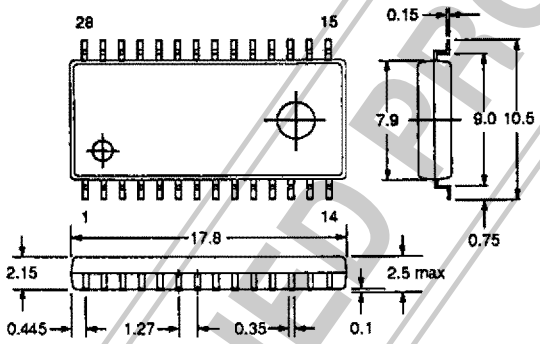
3012A-DIP28

[LC7883K]

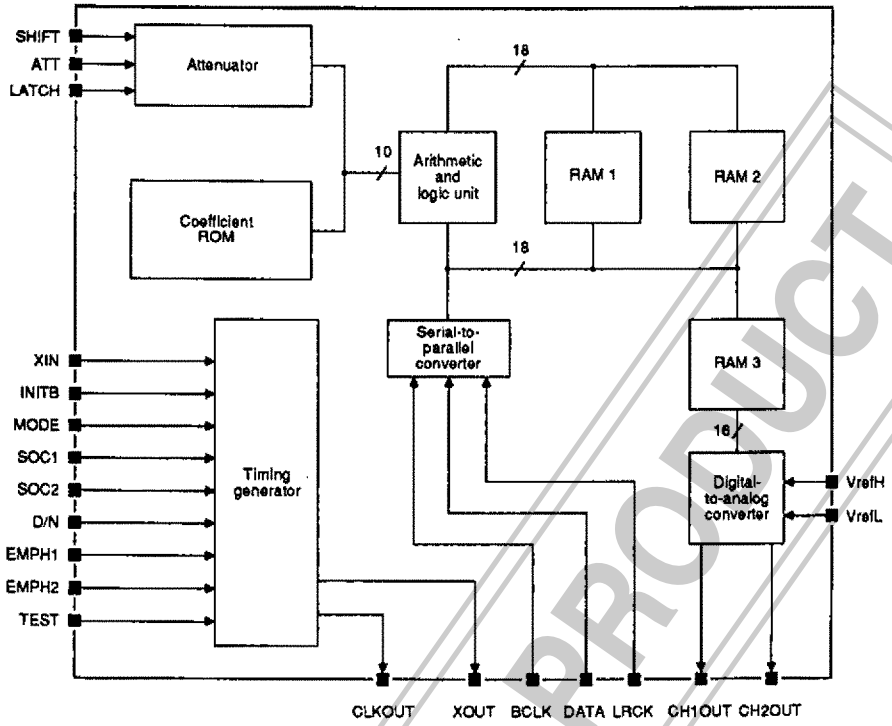


3091-MFP28

[LC7883KM]



Block Diagram



Pin Functions

Number	Name	Function
1	CH1OUT	Digital-to-analog converter channel 1 output
2	VrefH	HIGH-level reference voltage
3	AVDD	Analog circuit power supply
4	DVDD	Digital circuit power supply
5	BCLK	Serial bit-clock input
6	DATA	Digital-audio serial data input
7	LRCK	Channel select clock input
8, 13	TEST	Test inputs. Normally LOW
9	ATT	Attenuator and control data serial input
10	SHIFT	Attenuator and control data shift clock input
11	LATCH	Attenuator and control data latch input
12	INITB	Initialization input. Normally HIGH
14	EMPH2	Deemphasis select inputs
15	EMPH1	
16	D/N	Double/normal sampling frequency select input
17	SOC2	Source select inputs with internal pull-down
18	SOC1	
19	MODE	Operating mode select input with internal pull-down
20, 21	TEST	Test inputs with internal pull-down. Normally LOW

Number	Name	Function
22	DGND	Digital ground
23	CLKOUT	Clock output
24	XIN	Crystal oscillator input
25	XOUT	Crystal oscillator output
26	AGND	Analog ground
27	VrefL	LOW-level reference voltage
28	CH2OUT	Digital-to-analog converter channel 2 output

Specifications

Absolute Maximum Ratings at Ta = 25 °C, V_{SS} = 0 V

Parameter	Symbol	Ratings	Unit
Supply voltage range	V_{DD} max	–0.3 to 7.0	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Output voltage range	V_{OUT}	–0.3 to V_{DD} + 0.3	V
Operating temperature range	Topr	–30 to +75	°C
Storage temperature range	T_{stg}	–40 to +125	°C

Allowable Operating Ranges

T_a = 25 °C

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	5	V
Supply voltage range	V_{DD}	4.5 to 5.5	V
LOW-level reference voltage	V_{refL}	0 to 0.5	V
HIGH-level reference voltage	V_{refH}	V_{DD} – 0.5 to V_{DD}	V

Electrical Characteristics

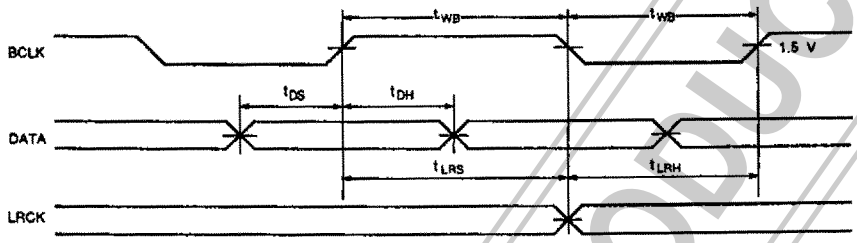
V_{DD} = 5.0 V, T_a = 25 °C, V_{refL} = 0 V, V_{refH} = 5.0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
LOW-level input voltage	V_{IL}		–0.3	–	+0.8	V
HIGH-level input voltage	V_{IH}		2.2	–	V_{DD} + 0.3	V
DAC resolution	RES		–	16	–	bits
Total harmonic distortion	THD	1 kHz, 0 dB	–	–	0.08	%
Crosstalk	CT	1 kHz, 0 dB	–	–85	–79	dB
Signal-to-noise ratio	S/N	1 kHz, 0 dB	85	92	–	dB
Power dissipation	P_d	XIN amplitude = 1.5 to 3.5 V, f_X = 16.9344 MHz	–	250	300	mW
Crystal oscillator frequency	f_X		–	16.9344	25	MHz

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Bit-clock input frequency	f_{BCX}		–	–	3.1	MHz
Internal pull-down resistance	R_{DOWN}		10	–	80	kΩ

Timing Characteristics

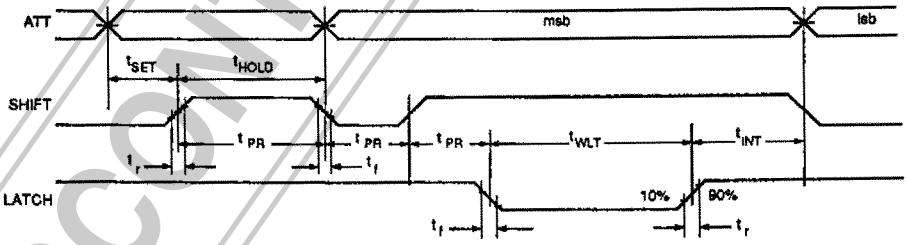
Audio input timing



V_{DD} = 5.0 V, T_a = 25 °C, V_{refL} = 0 V, V_{refH} = 5.0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Bit-clock input pulsewidth	t_{WB}		100	–	–	ns
Input data setup time	t_{DS}		20	–	–	ns
Input data hold time	t_{DH}		20	–	–	ns
Channel select clock input setup time	t_{LRS}		50	–	–	ns
Channel select clock input hold time	t_{LRH}		50	–	–	ns

Control input timing



V_{DD} = 5.0 V, T_a = 25 °C, V_{refL} = 0 V, V_{refH} = 5.0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Control input reference time	t_{PR}	f_X = 16.9344 MHz	250	–	–	ns
Latch input pulsewidth	t_{WLT}		50	–	–	ns
Shift clock and latch pulse input rise time	t_r		–	–	200	ns
Shift clock and latch pulse input fall time	t_f		–	–	200	ns

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Attenuator setup time	t_{SET}		500	–	–	ns
Attenuator hold time	t_{HOLD}		500	–	–	ns
Interval	t_{INT}		1000	–	–	ns

Functional Description

Theoretical Filter Characteristics

The theoretical filter characteristic for 40 dB or higher attenuation and passband ripple to within ±0.05 dB for normal-rate, eight-times over-sampling, is shown in figure 1, and for double-rate, four-times over-sampling, in figure 2.

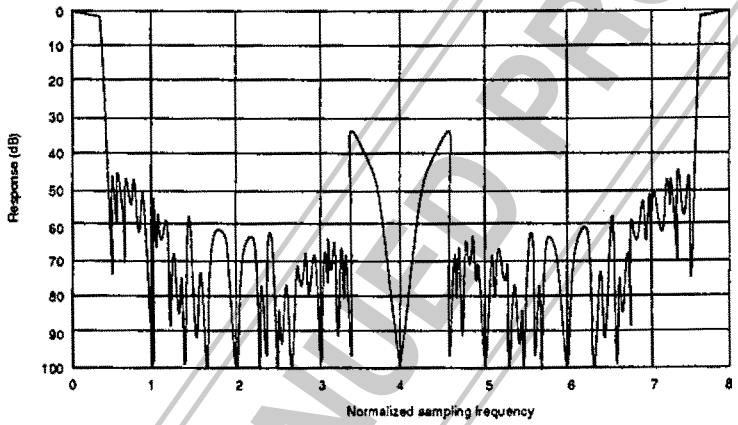


Figure 1. Normal-rate sampling filter characteristic

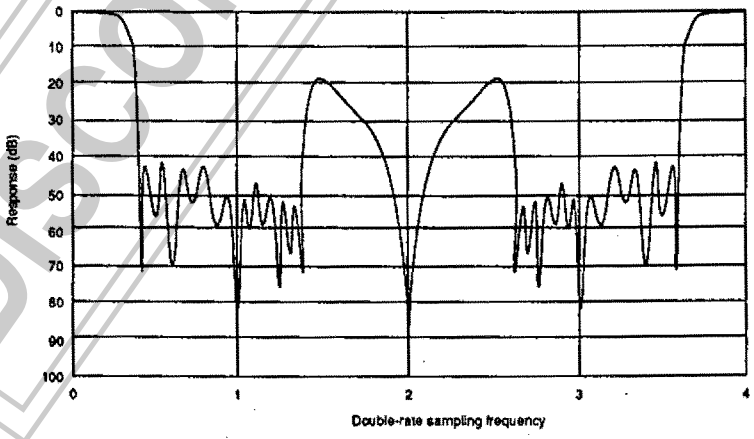


Figure 2. Double-rate sampling filter characteristic

Note that the sampling frequency, F_s, is double the input frequency.

Input Data Format

Serial data is input in 2s complement format with the most significant bit (msb) first. Control data is input with the least significant bit (lsb) first, as shown in figure 3.

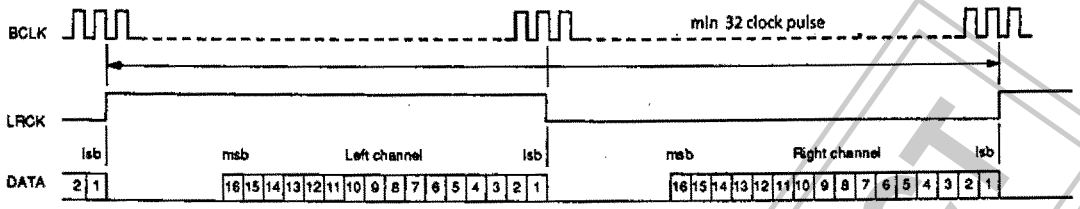


Figure 3. Input data format

Digital Filter

The block diagram of the digital filter is shown in figures 4 and 5. Data is transferred between the filter arithmetic blocks as 18-bit words. The final filter block uses the lower 6 bits to perform noise shaping and outputs a 16-bit word to the D/A converter.

The filter can operate in either normal-rate or double-rate mode. In normal-rate mode, each finite-impulse-response (FIR) filter doubles the sampling rate of the signal to produce an eight-times over-sampled signal. Deemphasis is performed by the infinite-impulse-response (IIR) filter.

Double-rate mode is typically used for high-speed dubbing from CD to tape. The input frequency on XIN is the same as for normal-rate processing, but the BCLK, DATA, and LRCK signals operate at twice the normal rate. Two FIR filters output a four-times over-sampled signal.

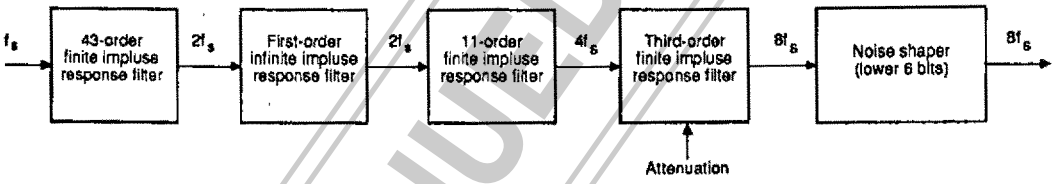


Figure 4. Normal-rate mode filter

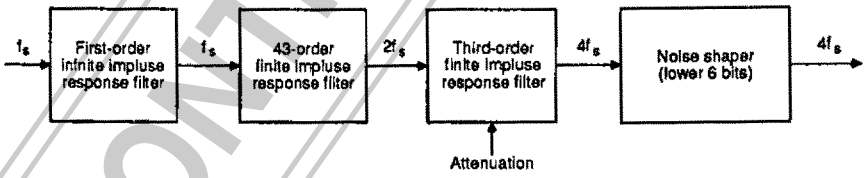


Figure 5. Double-rate mode filter

Digital-to-analog Converter

The LC7883K D/A converter is identical to that of the LC7881. Each channel contains a dynamic level shifter comprising three stages—a resistor-string D/A converter, a PWM D/A converter and a level-shifting D/A converter.

Initialization

When power is applied or the input source is changed, the LC7883K should be re-initialized. The supply to XIN, BCLK and LRCK should be connected only after the supply has stabilized, and INITB should be held LOW for at least one period of the LRCK signal, as shown in figure 6.

Note that the LC7883K should be re-initialized if the input data format fails. This may occur during channel selection if LRCK slips out of phase or if the digital input phase relationships change.

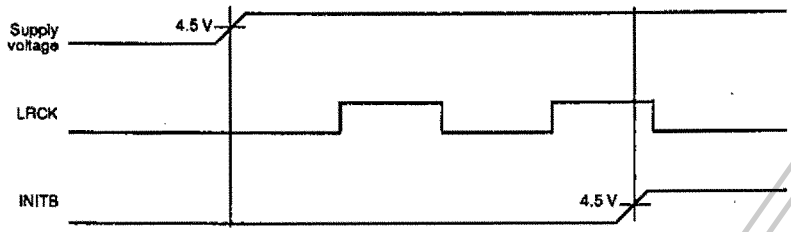


Figure 6. Initialization

Selection of Input Source

The SOC1 and SOC2 inputs should be set according to the required clock frequency as shown in table 1. Channel 1 is selected when LRCK is HIGH, and channel 2, when LRCK is LOW.

Table 1. Clock frequency selection

SOC1	SOC2	Clock frequency
LOW	LOW	$384F_s$
LOW	HIGH	$392F_s$
HIGH	LOW	$448F_s$
HIGH	HIGH	$512F_s$

Mode Selection

When MODE is HIGH, deemphasis and the sampling rate can be selected using EMPH1 and EMPH2 as shown in table 2. These parameters can also be selected using serial control data.

Table 2. Deemphasis and sampling rate selection

EMPH1	EMPH2	Deemphasis	Sampling rate
LOW	LOW	OFF	–
LOW	HIGH	ON	32 kHz
HIGH	LOW	ON	44.1 kHz
HIGH	HIGH	ON	48 kHz

Normal-rate sampling is selected when D/N is LOW, and double-rate sampling, when D/N is HIGH. The ATT, SHIFT and LATCH inputs should be held stable at a single logic level while MODE is HIGH.

Control input data mode is selected when MODE is LOW. Control data is input on ATT. The EMPH1, EMPH2 and D/N inputs should be held stable at a single logic level while MODE is LOW.

Control Data Format

The control data has the format shown in figure 7. The control data comprises deemphasis and normal/ double-rate select bits, and the digital attenuator coefficient.

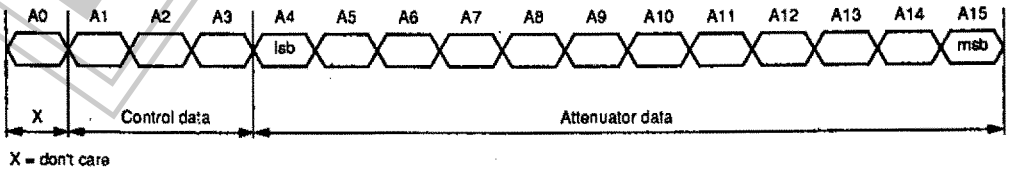


Figure 7. Control data format

Normal rate is selected when A1 is LOW, and double rate, when A1 is HIGH. Deemphasis filtering is selected using A2 and A3 as shown in table 3.

Table 3. Deemphasis filtering

A2	A3	Deemphasis	Sampling rate
LOW	LOW	OFF	–
LOW	HIGH	ON	32 kHz
HIGH	LOW	ON	44.1 kHz
HIGH	HIGH	ON	48 kHz

Upon initialization, the attenuator data is set to 4000H (only A14 is set).

Bits A4 to A15 are the attenuator multiplier coefficient. As the attenuator multiplier is only a 10-bit coefficient, only the upper 10 bits (A6 to A15) are used to select the attenuation. The attenuation is given by the following equation.

Attenuation = –20 log ((Upper 10 bits) / 256) dB

If the upper 10 bits are all zero, then bits A4 and A5 are used to select the attenuation as shown in table 4.

If the attenuation data is changed, the attenuation is changed by one step each sample period. For example, if the attenuator data is changed from 400H to 000H, the change in attenuation occurs over an interval of $1024/F_s$ seconds.

Table 4. Attenuation

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	Attenuation (dB)
0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	1	1	1	1	1	0.034
0	0	1	1	1	1	1	1	1	1	1	0	0.034
0	0	1	1	1	1	1	1	1	1	0	1	0.034
0	0	1	1	1	1	1	1	1	1	0	0	0.034
0	0	1	1	1	1	1	1	1	0	1	1	0.068
0	0	1	1	1	1	1	1	1	0	1	0	0.068
to												
0	0	0	0	0	0	0	0	0	1	0	0	48.16
0	0	0	0	0	0	0	0	0	0	1	1	50.66
0	0	0	0	0	0	0	0	0	0	1	0	54.19
0	0	0	0	0	0	0	0	0	0	0	1	60.21
0	0	0	0	0	0	0	0	0	0	0	0	∞

Typical Application

Note

The digital-to-analog converters have high impedance outputs, which can be matched using emitter follower op-amps. The TEST pins are normally tied LOW, and INITB, HIGH.

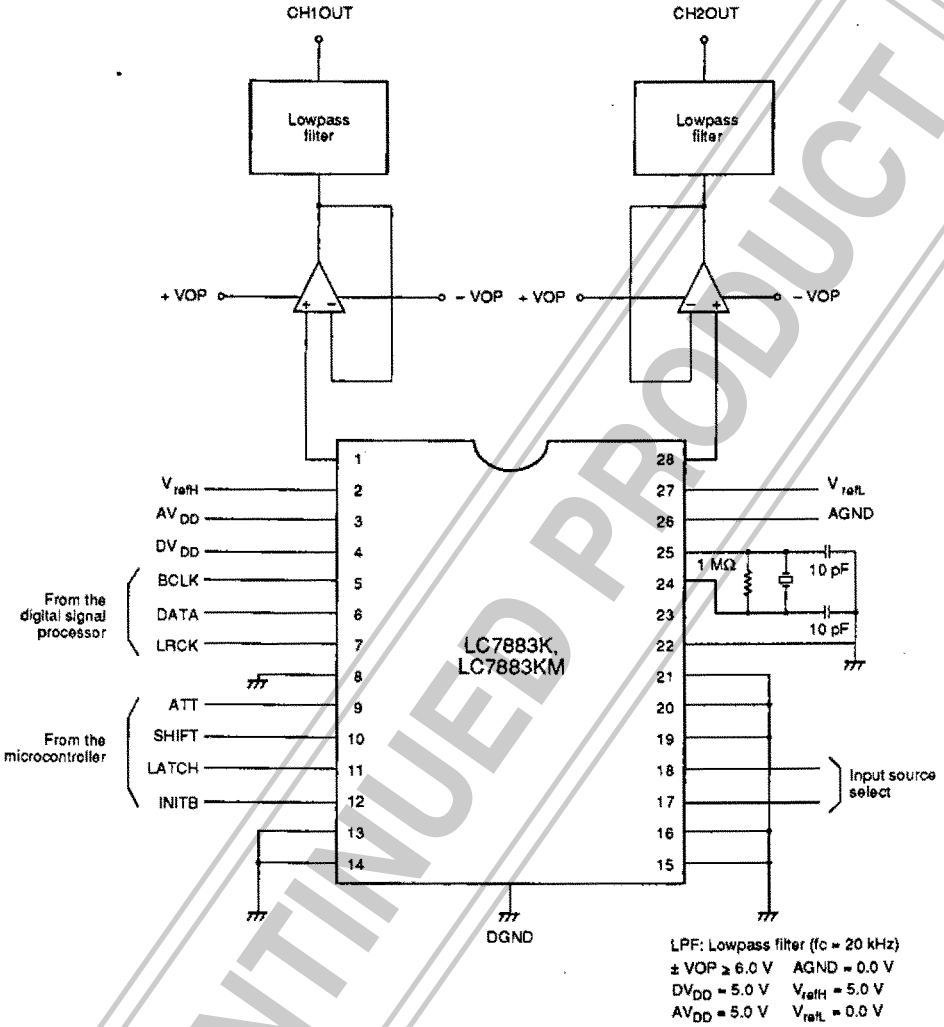


Figure 8. Typical application